

SILEX MICROSYSTEMS

YOUR PURE PLAY
MEMS FOUNDRY

Silex Microsystems
A US perspective



Silex - a Pure Play MEMS Foundry

- **Pure Play MEMS Foundry**
 - Application agnostic
 - Volume production of MEMS
 - More than 100 customized products
- **Leadership in MEMS foundry services**
 - New advanced MEMS 8" wafer fab
 - State-of-the-art 6" MEMS wafer fab
 - Deployment of standard process platforms
- **Strong customer base**
 - 80 international customers
 - 10 in volume production
- **Key Facts**
 - Founded 2000
 - 2010 Net Sales \$37 million
 - Number of employees ~140



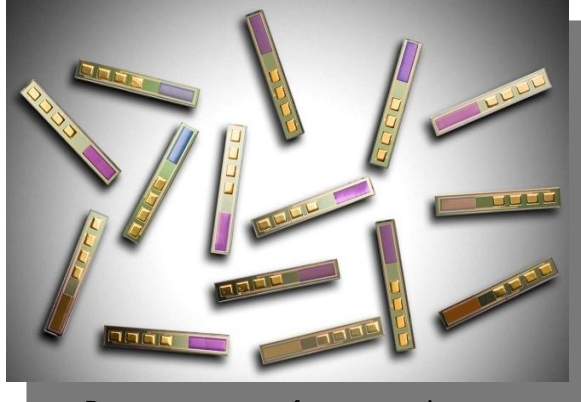
MEMS Foundry Business

- Majority of new MEMS activities are fabless
- Wafer fab is large investment with significant fixed costs
- MEMS wafer volumes inherently small
- Success is depending on foundry know-how and expertise
- Important MEMS foundry selection criteria:
 - Flexibility and full understanding of true MEMS processing
 - Solid business model and expansion capability
 - Quality assurance
 - Protection of IP & know-how
- Shorter time to market
 - Standard process platforms to mitigate risk and lower total cost

Silex Foundry Strategy

- **Explicit "PURE PLAY FOUNDRY" strategy – No own products**
- **Target customers have products that hold potential for volume production**
- **Fully equipped MEMS fab, leading engineering expertise and experience from manufacturing a wide range of MEMS products**
- **Proprietary foundry process platforms, leveraging intellectual property and know-how**
- **Continue to expand manufacturing capacity founded on customer demands**
- **High quality and cost efficient manufacturing**

MEMS Produced by Silex



Pressure sensors for measuring blood pressure in coronary arteries

Mirrors for optical switching

Accelerometers

Gyros

Pressure Sensors

Cantilevers

Touch Membranes

Flow Sensors

Filter Structures

CMOS Interposers

Needles

Cell Analysis

Microphones

RF components

Lab-on-Chips

Print Heads

**Drug Delivery
Devices**

Mirrors

Optical Benches

2011 - MEMS Foundry Challenges

- Majority of MEMS components are not using standardized processes.
- While many process blocks are standardized the combination of process blocks are still unique (and the standardization is internal per each Foundry).
- Silex uses both standardized process block (for example Sil-VIA®) as well as standardized process platforms.
- Customers insist on “violating” at least one design rule/advice which causes the need for customization remains.
- Local support is not necessary but is an advantage.
- Pure play MEMS foundries still a small part of total MEMS manufacturing.

Silex situation:

- Silex expects to be ranked number 1-3 of pure play MEMS Foundries for 2010.

2004 – MEMS Foundry Challenges

- **Virtually no MEMS components were using standardized processes.**
- **Almost no standard process blocks exists.**
- **Local support to large extent necessary.**

Silex situation:

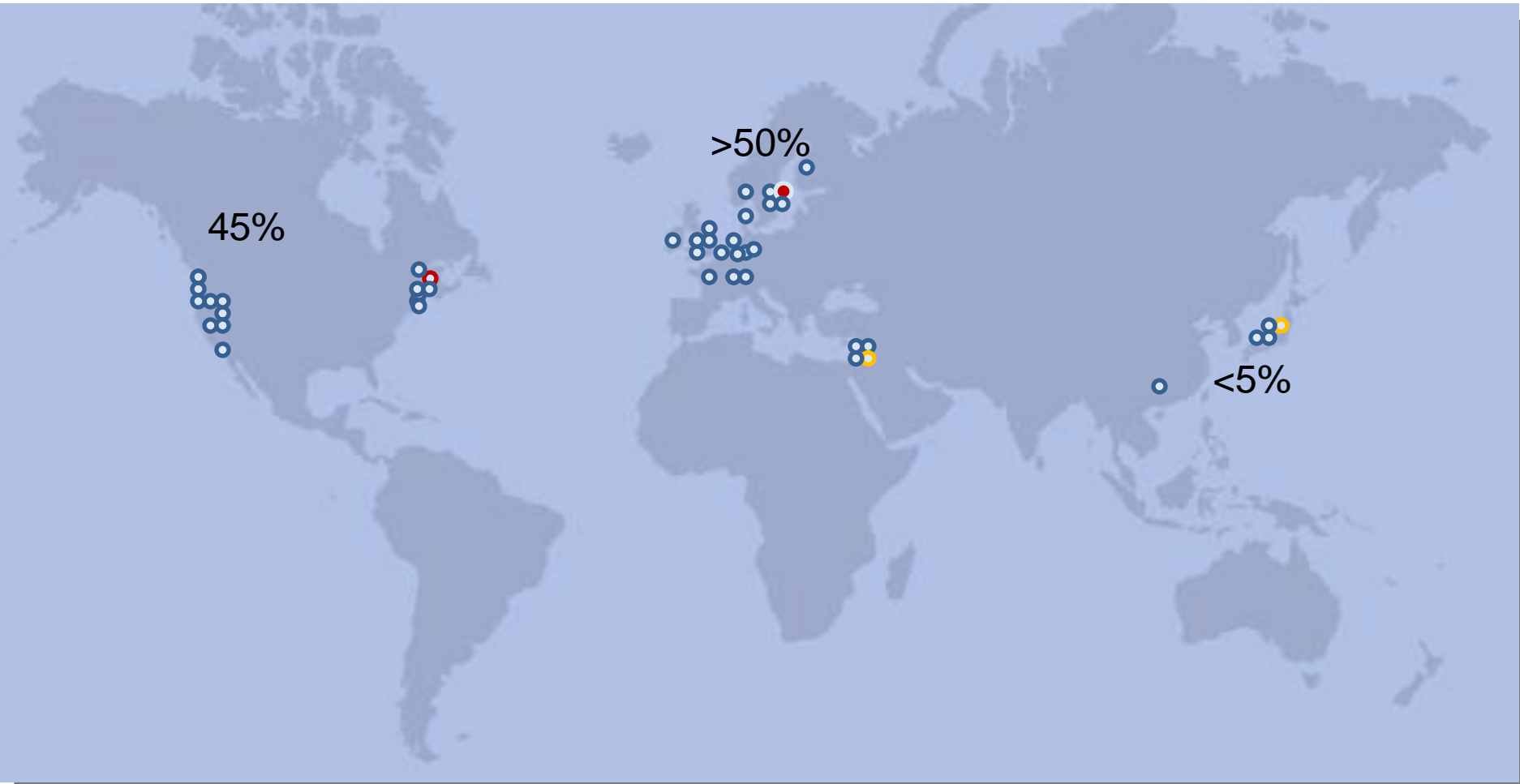
- **Silex first fab (6 inch) is brand new. Work on standardization of first process block (Sil-VIA®) performed and plan for standardized process block and standardized process platforms exists but is not implemented.**
- **Silex is a Northern European Company with almost 50 % of the business in North America and growth plans.**
- **Local support with intimate understanding of capabilities as well as company culture deemed necessary.**

2002 - Customers World Wide



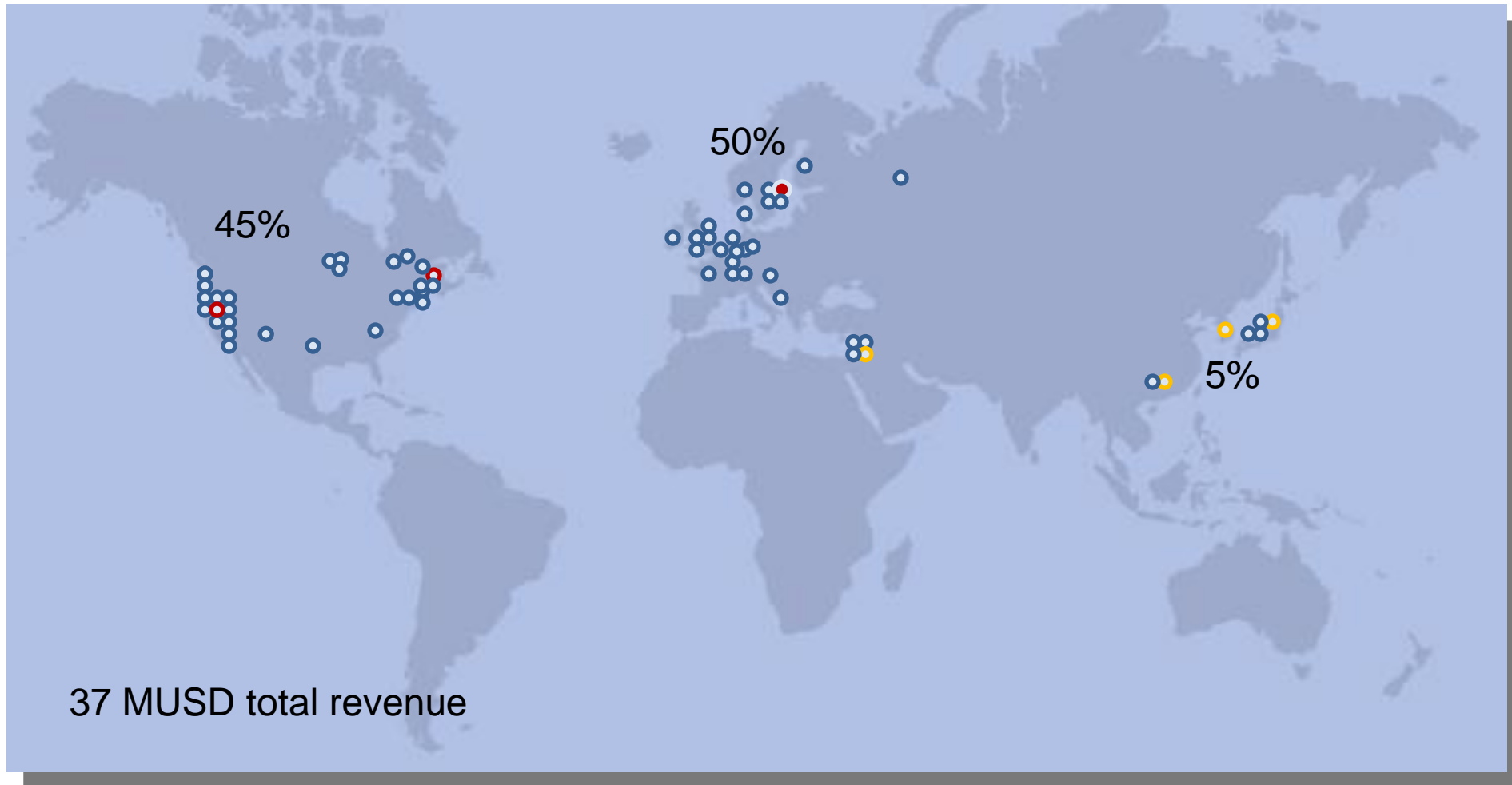
- Customer
- Headquarters
- Sales Office
- Agent

2005 - Customers World Wide



● Customer ● Headquarters ● Sales Office ● Agent

2010 - ~80 Customers World Wide



● Customer ● Headquarters ● Sales Office ● Agent

Establishing a local US entity

As a small high tech company costs are important:

- **Find some one that wants to go to US.**
- **Find a US lawyer that have done the same exercise before. Establish entity and transfer of first employee per L-1 status.**
- **Be amazed by the rules and regulations luckily to the largest extent handled by the lawyer/lawyers.**
- **The lawyers do cost.**

Some interesting situations to be prepared for:

- **As the US entity needs to be signed for before VISA is issued travel back and forward is necessary before employment can be transferred to the US entity.**
- **Without a credit record in US both the employee and the company needs to rely on “friends and family” relations.**

Considerations regarding local US entity

Location of first office, East Coast vs. West Coast:

Existing company cluster.

Company profile.

Distance to mother company.

Future business opportunities.

Circumstances.

Silex situation in 2004:

- **Largest customer cluster in Bay Area, 2nd largest in Boston area.**
- **With US “eyes” viewed ourselves as an East Coast company based on the Swedish location.**
- **West Coast 9 hour time difference, 12 hour flight.
East Coast 6 hour time difference, 7 hour flight.**
- **Largest business potential in the Bay Area.**
- **Mutual investors with a Boston company as well as private relations for employee to be transferred existed.**

=> Circumstances swayed for Boston area.

Silex local US entity

2005-2006:

- **1 employee, location Boston.**
- **Find a US lawyer that have done the same exercise before. Establish entity and transfer of first employee per L-1 status.**
- **Be amazed by the rules and regulations luckily to the largest extent handled by the lawyer/lawyers.**
- **The lawyers do cost.**

Some interesting situations to be prepared for:

- **As the US entity needs to be signed for before VISA is issued travel back and forward is necessary before employment can be transferred to the US entity.**
- **Without a credit record in US both the employee and the company needs to rely on “friends and family” relations.**

Silex local US entity

2011:

- **5 employees, locations Boston and Bay Area.**
- **First employee still active in company (now permanent US resident).**
- **Well established on US as well as international market.**
- **Recruiting for the Swedish entity on the US market.**

Manufacturing Facilities

- **6" Wafer fab (operational since 2004)**
 - 1200 m² clean room area class 10 -10 000
 - Capacity of 300.000 Litho-layers/year
 - Development and production coexist
 - ISO 9001:2008
 - 4 shift operation

- **8" wafer fab (operational since 2009)**
 - 1000 m² clean room area class 1-10
 - Capacity of 500.000 Litho-layers/year
 - Production focus
 - ISO 9001:2008
 - Sufficient capacity until end 2013



Motivation for 8"

- Increased capacity
- Reduced die cost (~30%)
- State-of -the-art equipment
- Integration with CMOS
- Wafer Level Capping

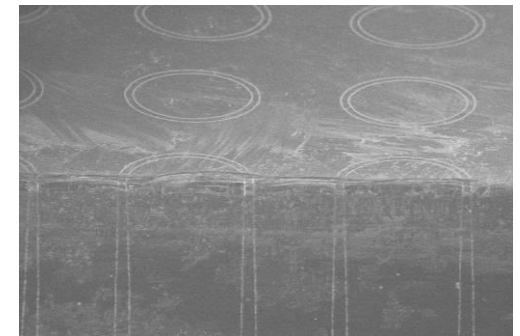
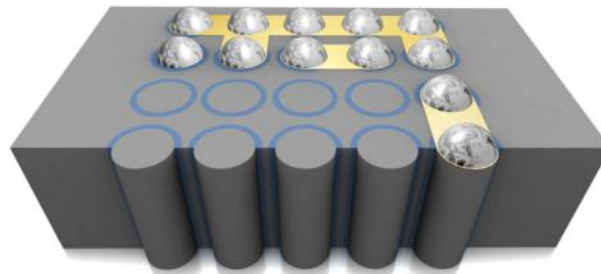


Targeting high volume consumer electronics, automotive and BioMEMS markets

MEMS Foundry Process Platforms

Sil-Via™ Process - Key Features & Advantages

- Small via pitch (<math><50 \mu\text{m}</math>) in thick substrates (600 $\mu\text{m}</math>)$
- "No metal" starting material with unrestricted post processing capability (high temperature processing up to 1100°C)
- Wafer level packaging of MEMS devices with vacuum sealing
- "All silicon package" for SMD assembly
- "Zero-Crosstalk" feature – isolating sections of die
- Contacting of CMOS wafer backside (EPI or SOI)

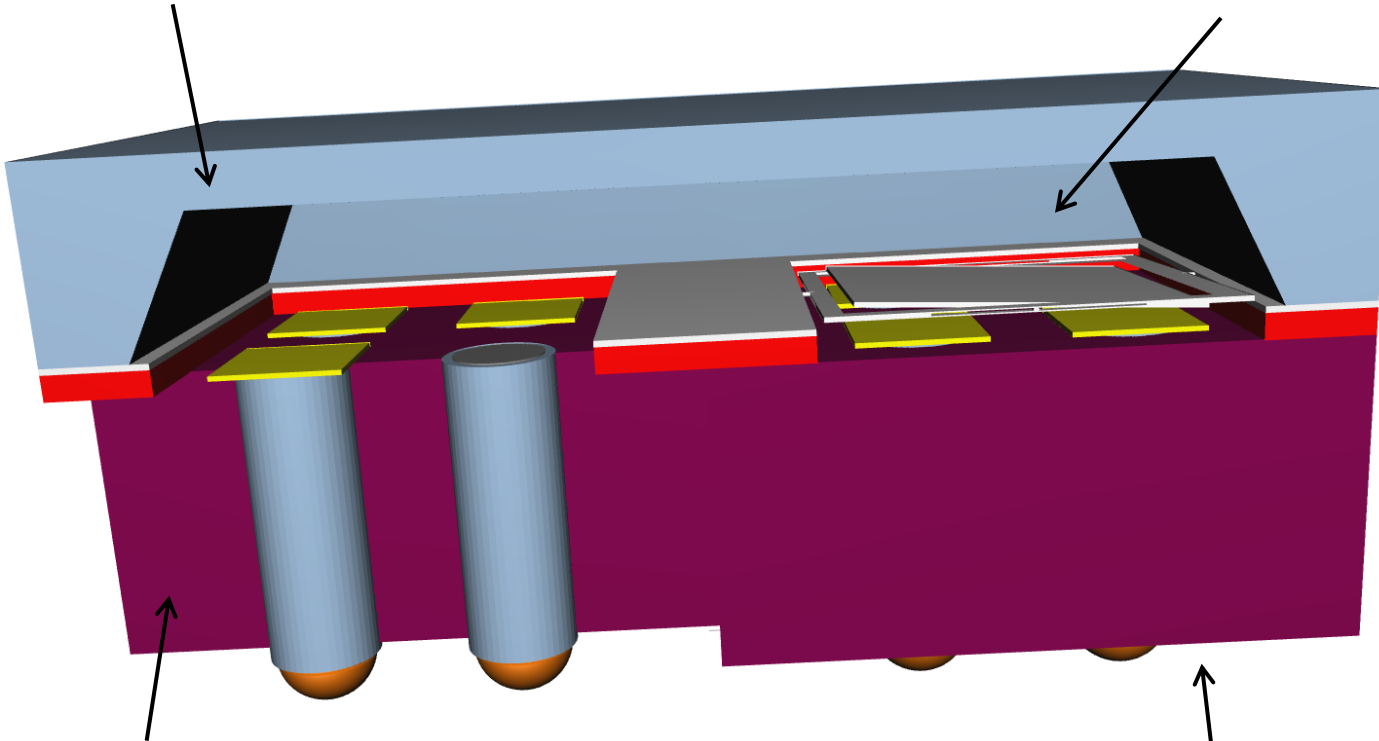


MEMS Foundry Process Platforms

- **Sil-Via™ - Through Silicon Via Process Platform**

Wafer level packaging of MEMS

Vacuum sealed cavity

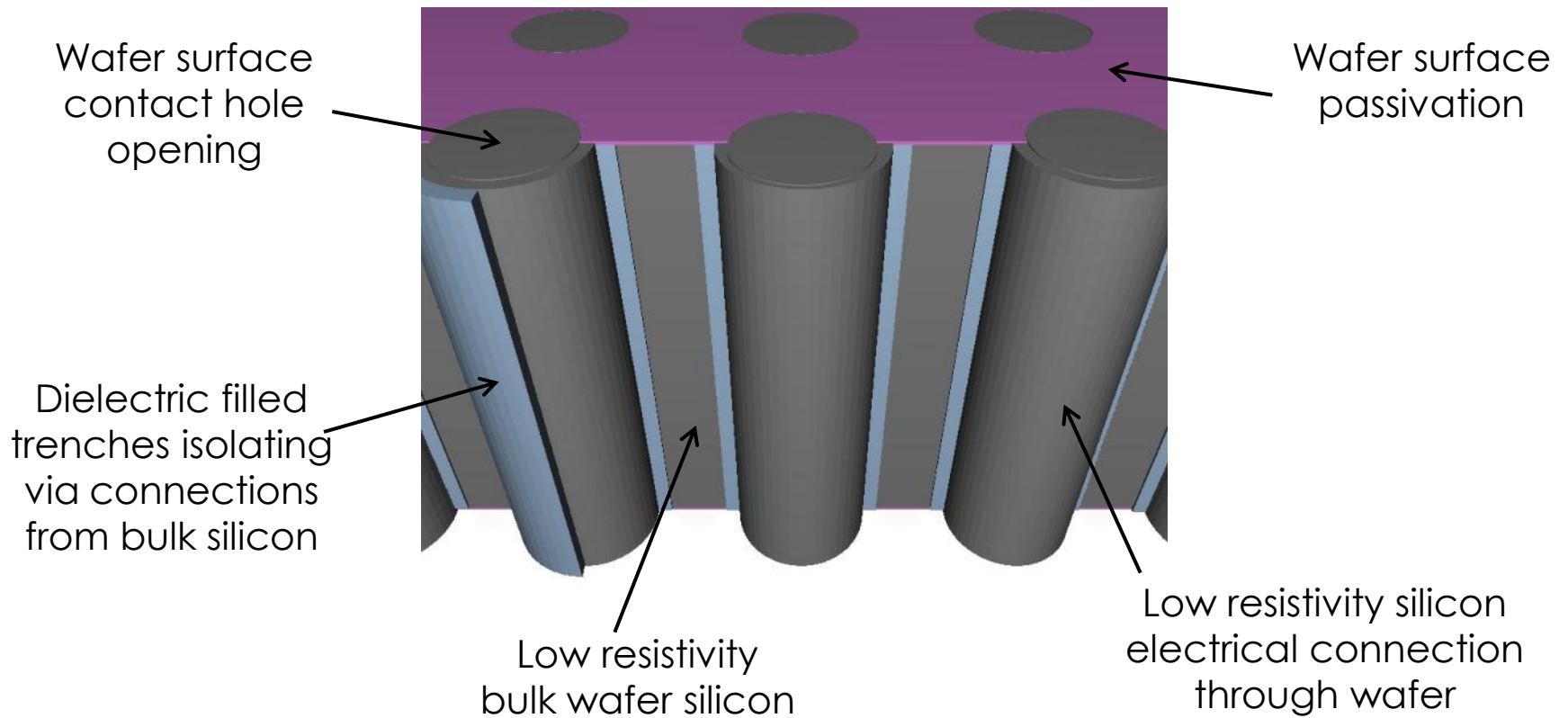


Unrestricted MEMS post processing of
via substrate (up to 1100°C)

“All silicon package”
mounted directly on PCB

MEMS Foundry Process Platforms

Sil-Via™ - Through Silicon Via Process Platform

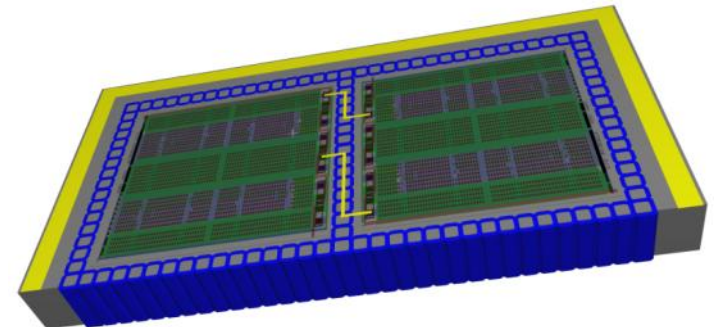
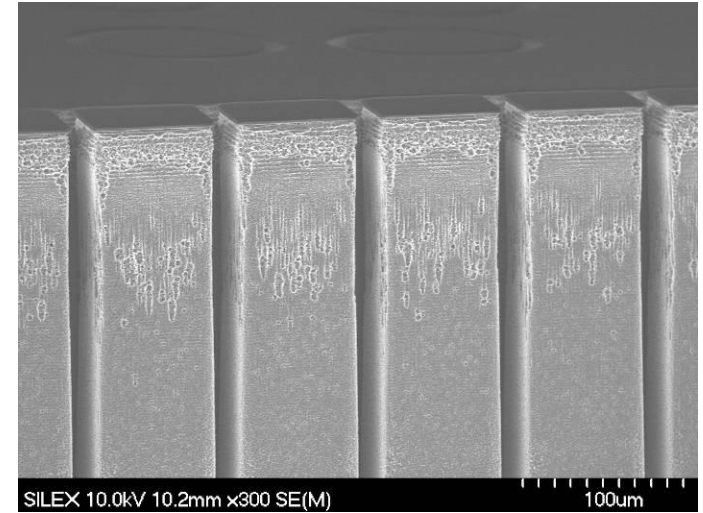
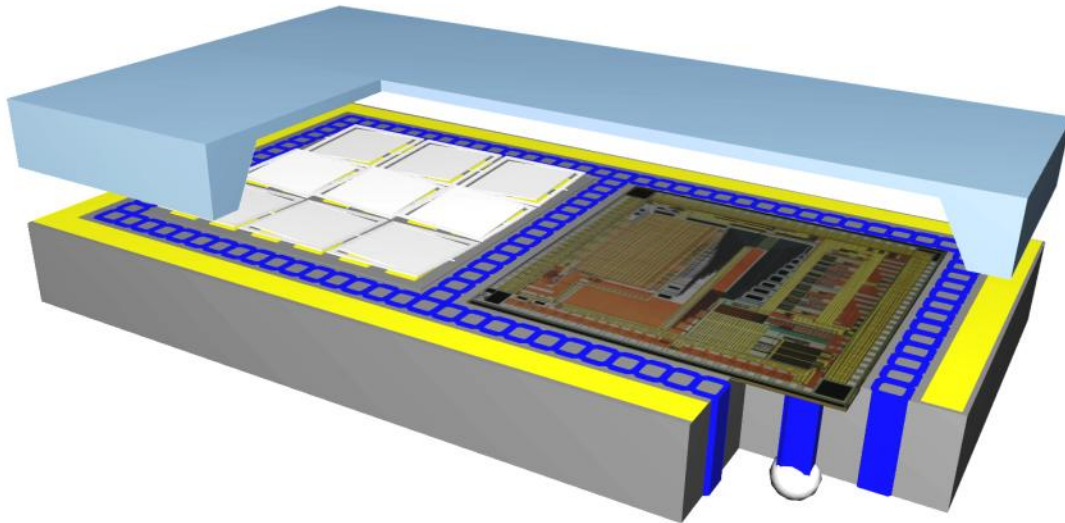


MEMS Foundry Process Platforms

“Zero Crosstalk” feature

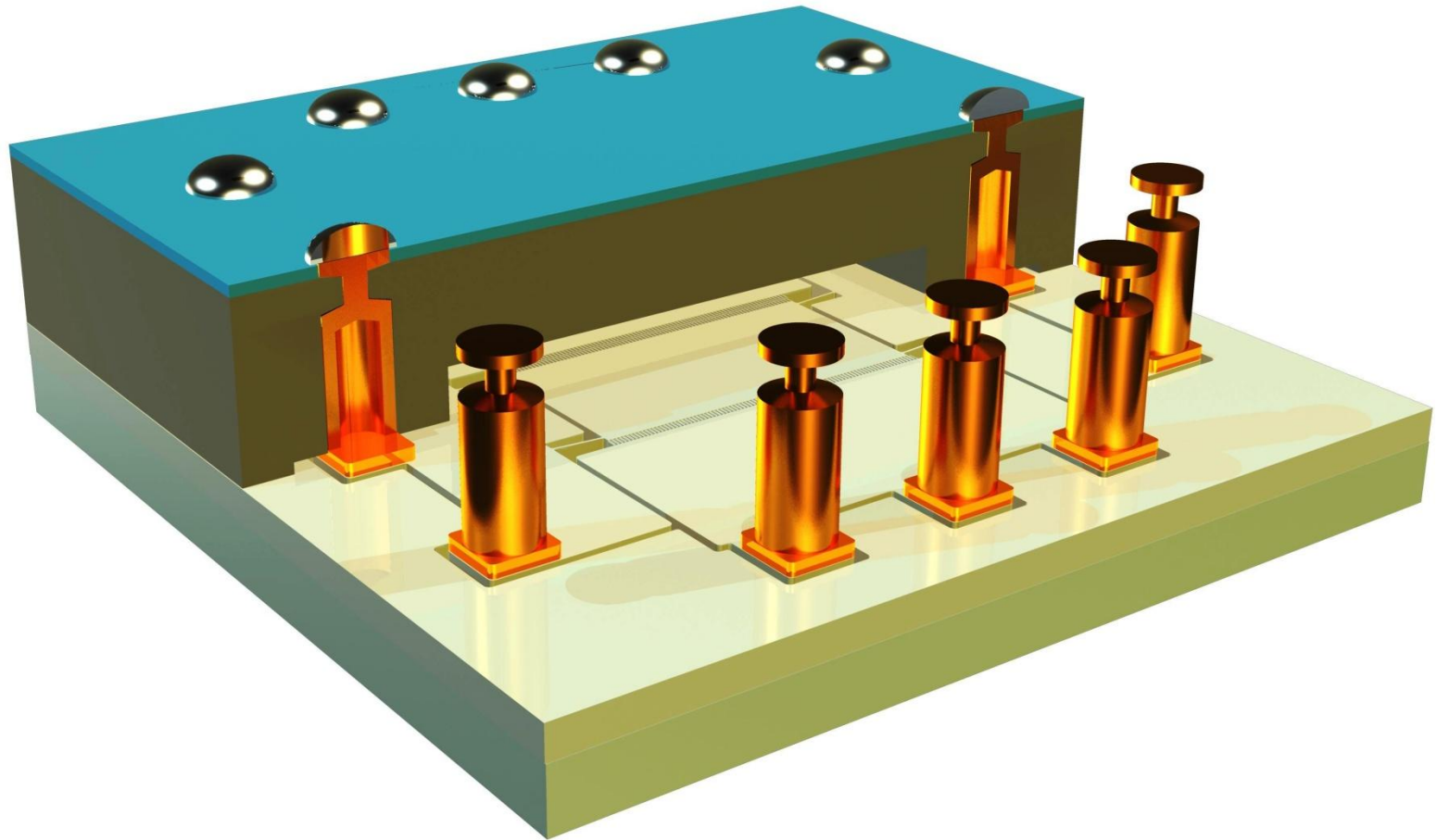
Reduced cross talk in mixed Signal IC's and MEMS

- Double trenches separate regions in mixed signal IC and MEMS dies

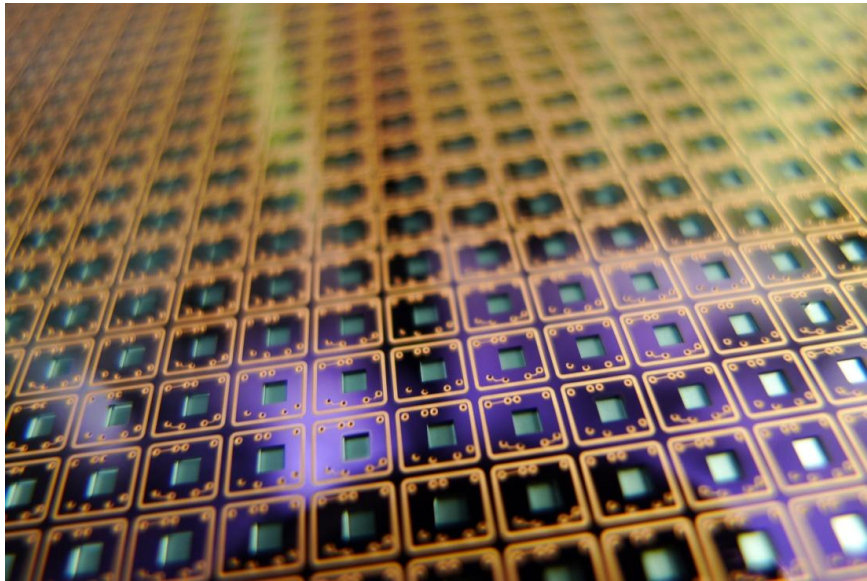


MEMS Foundry Process Platforms

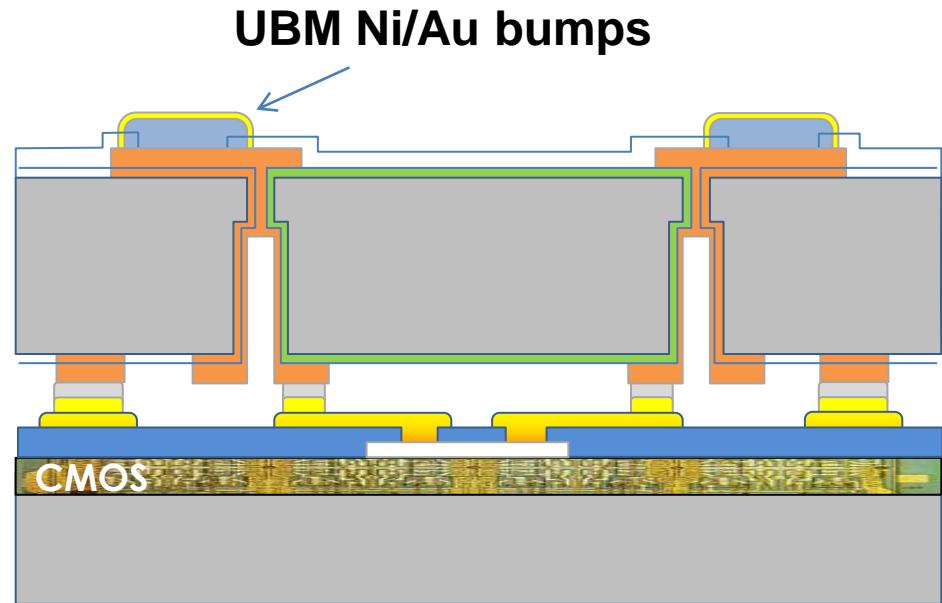
Met-Cap™ Process Platform



Met-Cap™ Process Platform

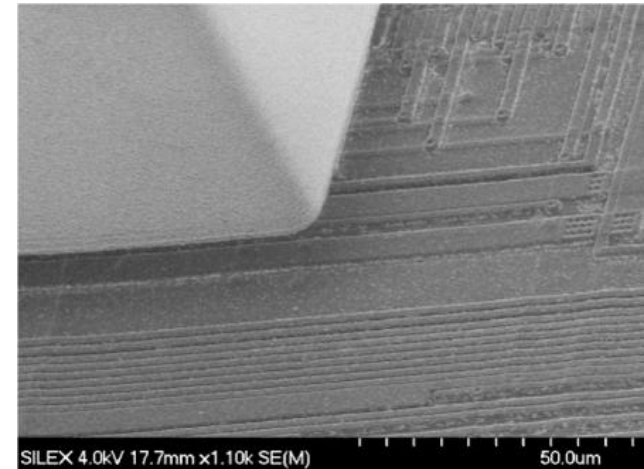
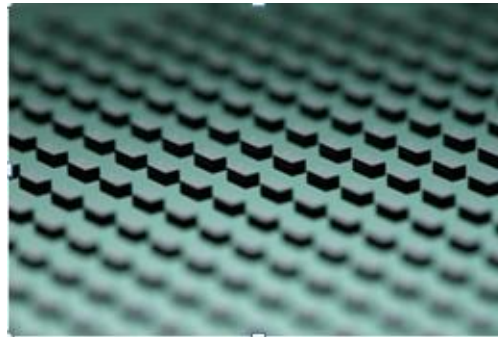
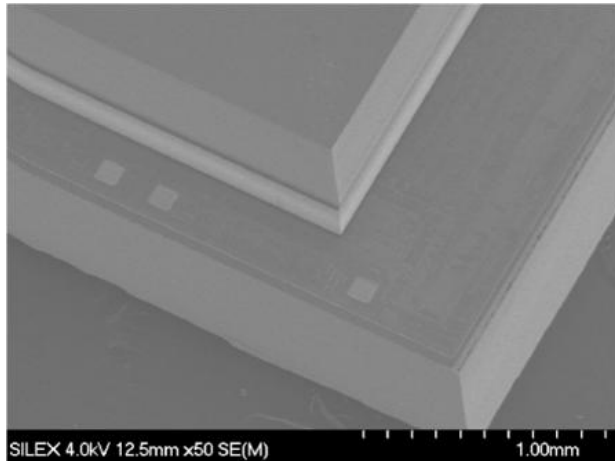


Top-view photo of Met-Cap™ before bonding



Cross-sectional view of Silex Met-Cap™ technology

Advanced Foundry Processes



- Bond to CMOS
- CMOS/MEMS release processing
- Wafer level capping

