Low Power Circuit Techniques for Energy Harvesting Applications

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Outline

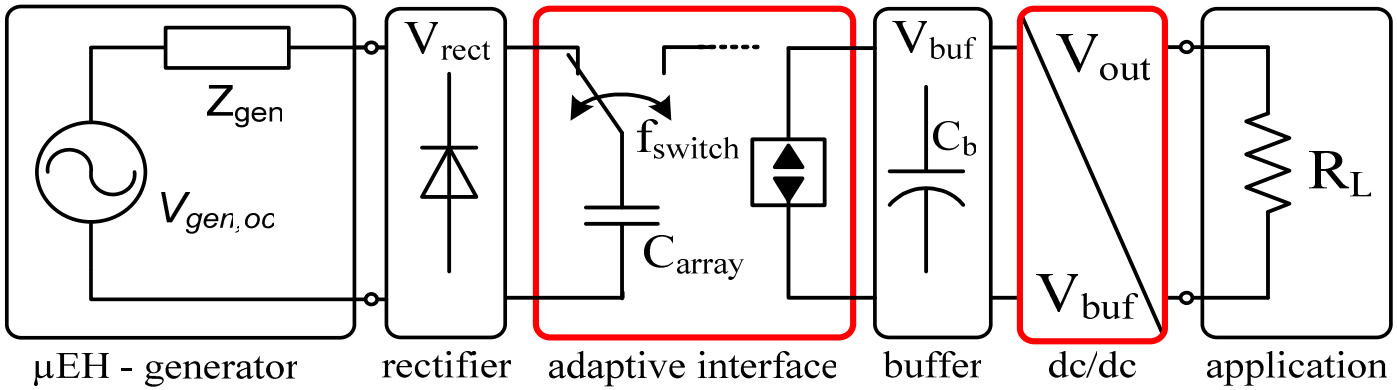
- Motivation: Two-Stage Power Processing
- Interface for Inductive Transducers
  - Operation Principle
  - Measurement Results
- Interface for Piezoelectric Transducers
  - Operation Principle
  - Measurement Results
- Low-Voltage Circuits and Converters
  - 0.5 V Amplifier
  - Comparator-less PWM
- Conclusion

Outline

- Motivation & Application Examples
- Rectification
  - Passive rectification
  - Active diodes
  - Floating gate enhanced CMOS-switches
- Interface for Electromagnetic Transducers
  - Load matching approach
  - Switched-capacitor converter
- Low-Voltage Circuits and Converters
  - 0.5 V amplifier
  - Comparator-less PWM

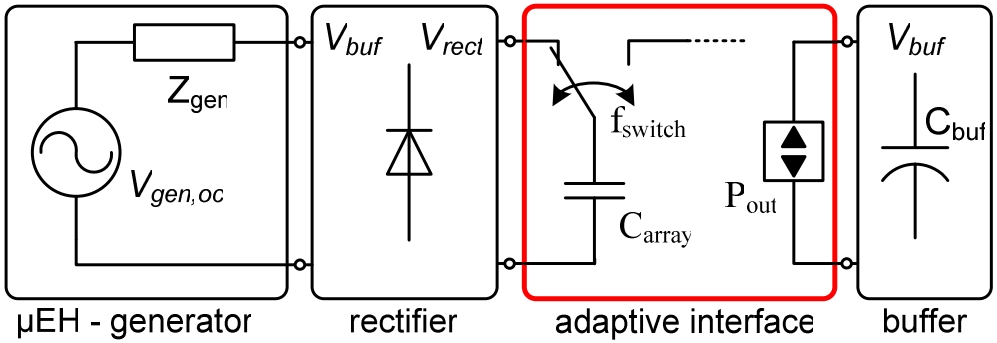
Two-Stage Power Processing

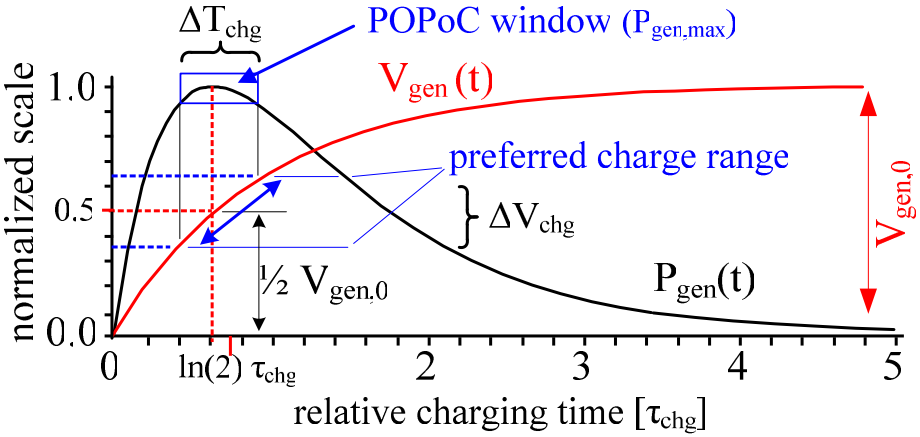
- Vibration energy harvesting (inductive – piezoelectric)
- 1st stage: generator interface for efficient harvesting



  - Load matching detection
  - Fluctuant buffer voltage
- 2nd stage: DC/DC voltage conversion
  - PWM control by modulated digital gate delays
  - Dedicated building blocks for low-voltage operation
  - Stable and controlled output voltage

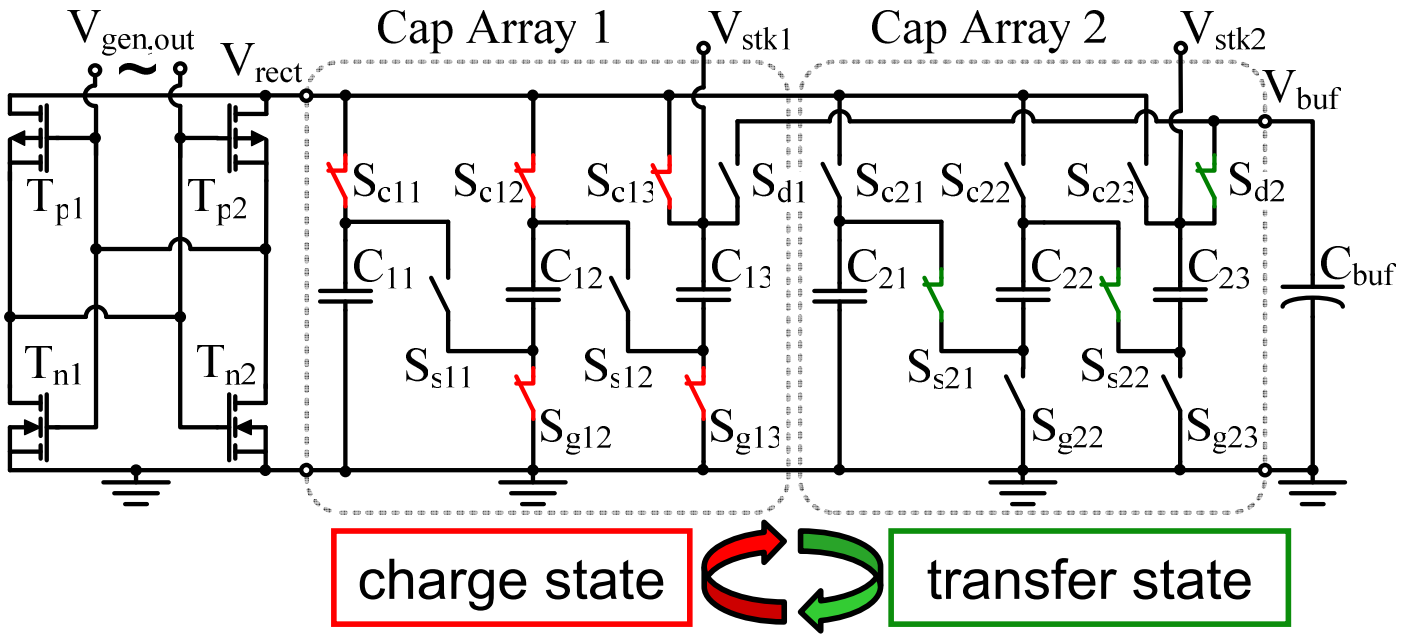
Adaptive Switched Capacitor Interface for Inductive Generators



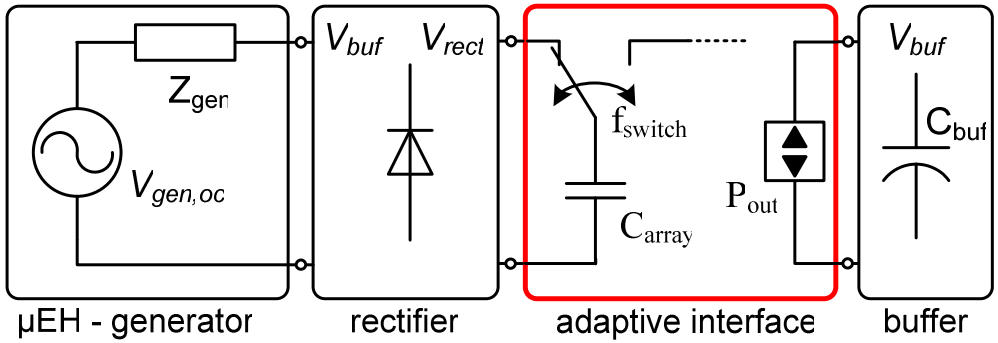


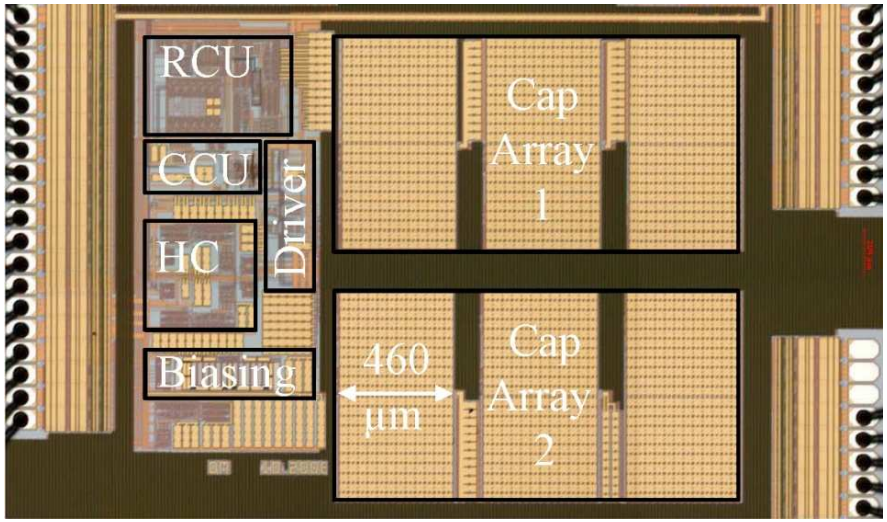
Requirement 1:
Load/ impedance matching

Requirement 2:
Independence of buffer voltage

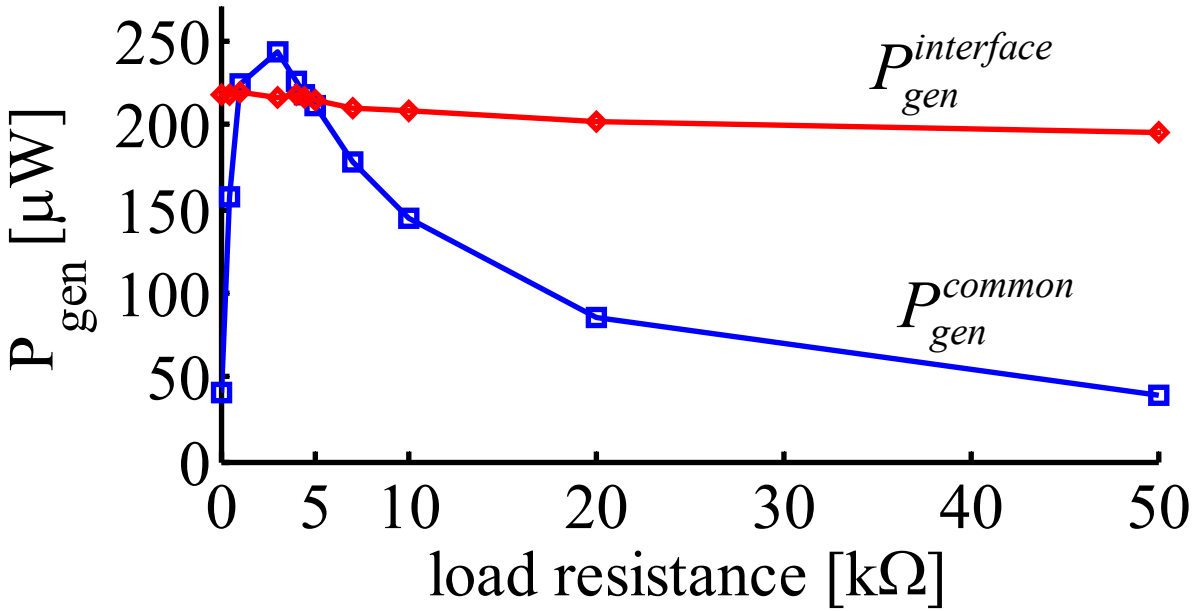


Adaptive Switched Capacitor Interface





[D. Maurath, ESSCIRC 2009]

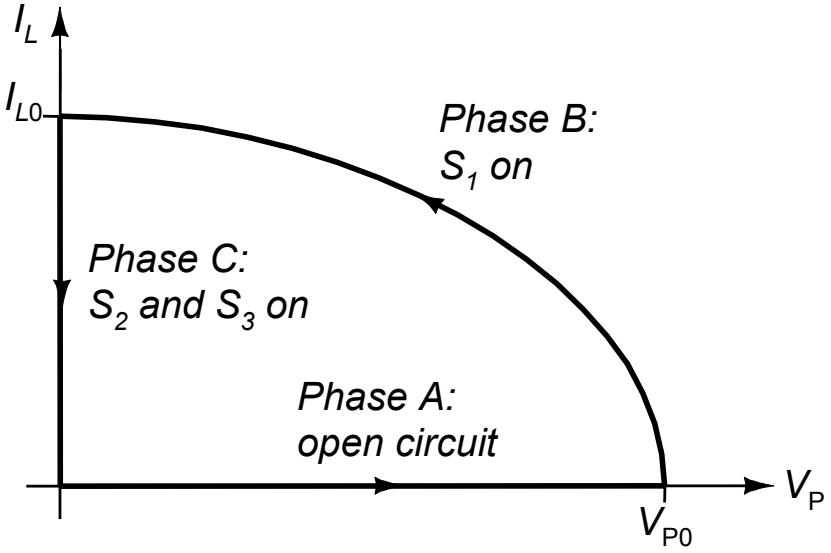


Generator parameters:

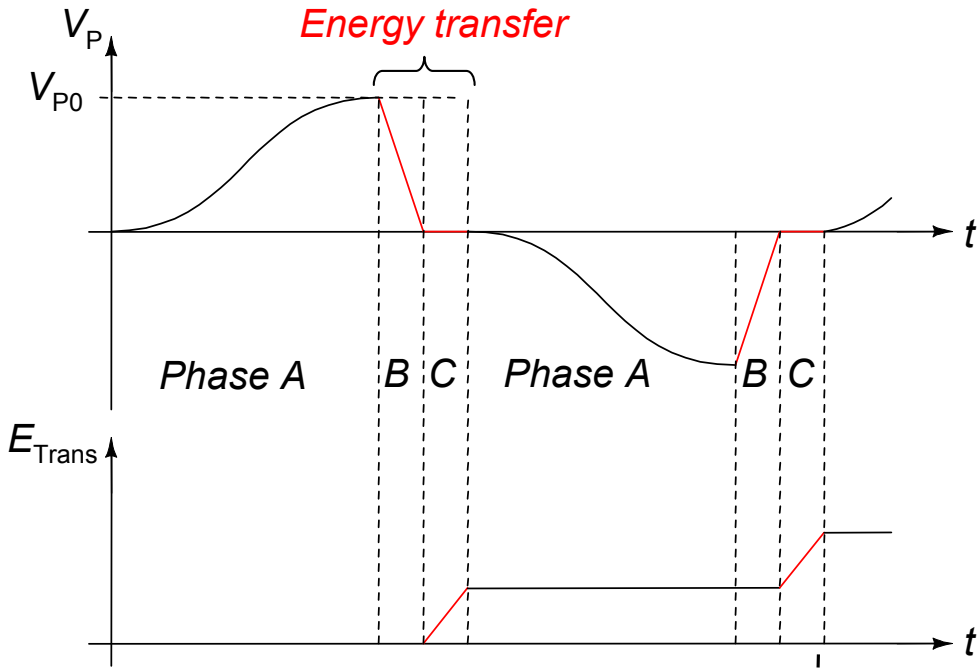
R_{gen}	2,05 kΩ
f_{res}	168 Hz
$V_{gen,0}^{peak}$	2.0 V
P_{max}	250 µW

Interface for Piezoelectric Generators

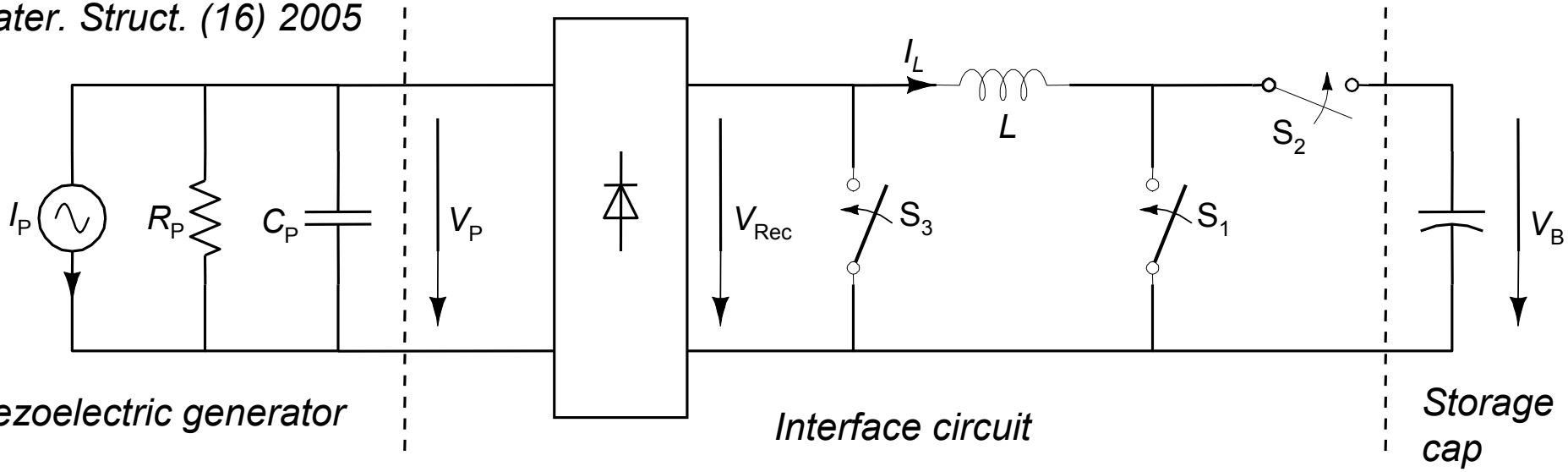
State diagram



Time diagram

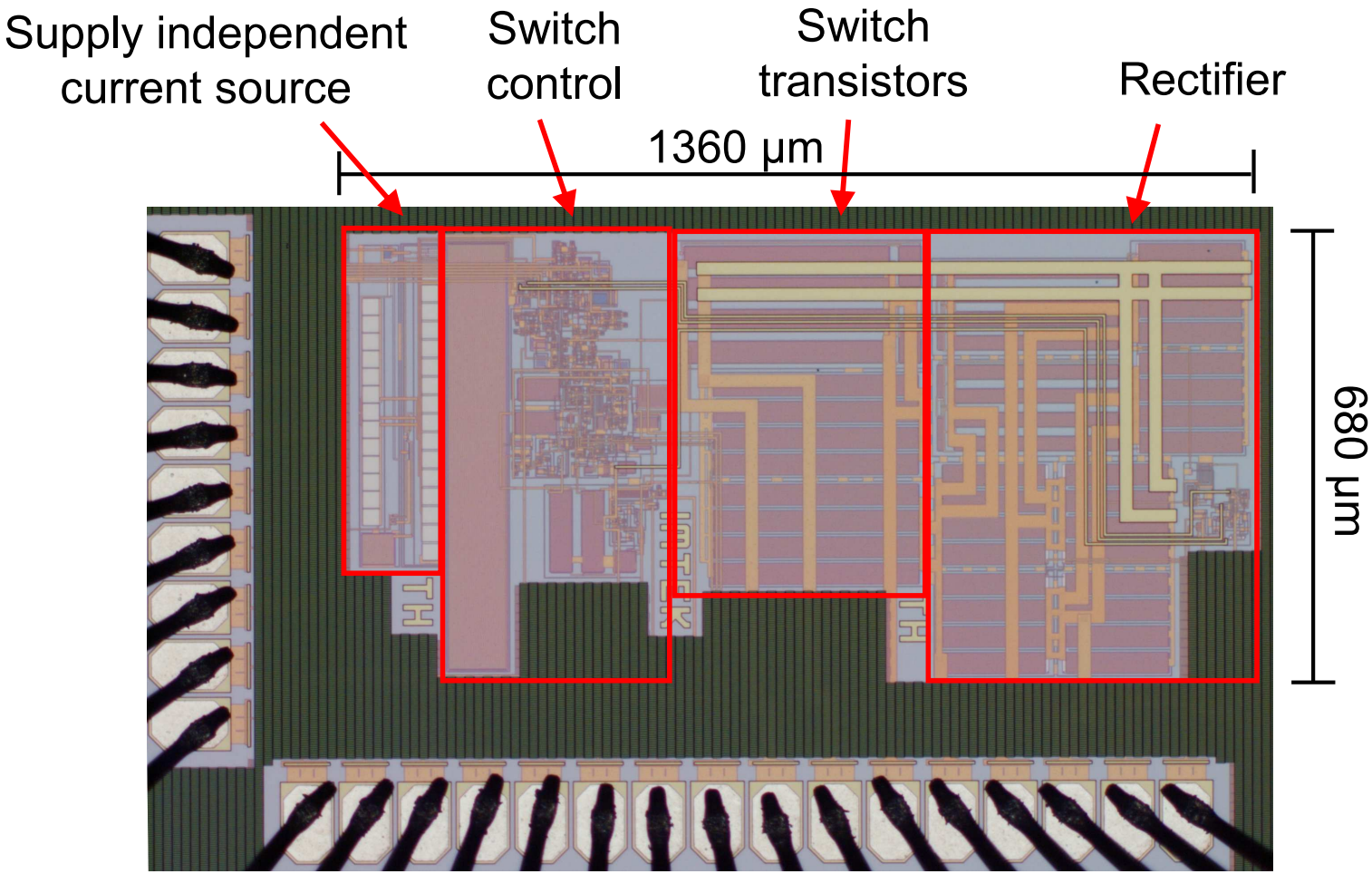


"Synchronous electric charge extraction", Lefeuvre et al., J. Int. Mater. Struct. (16) 2005

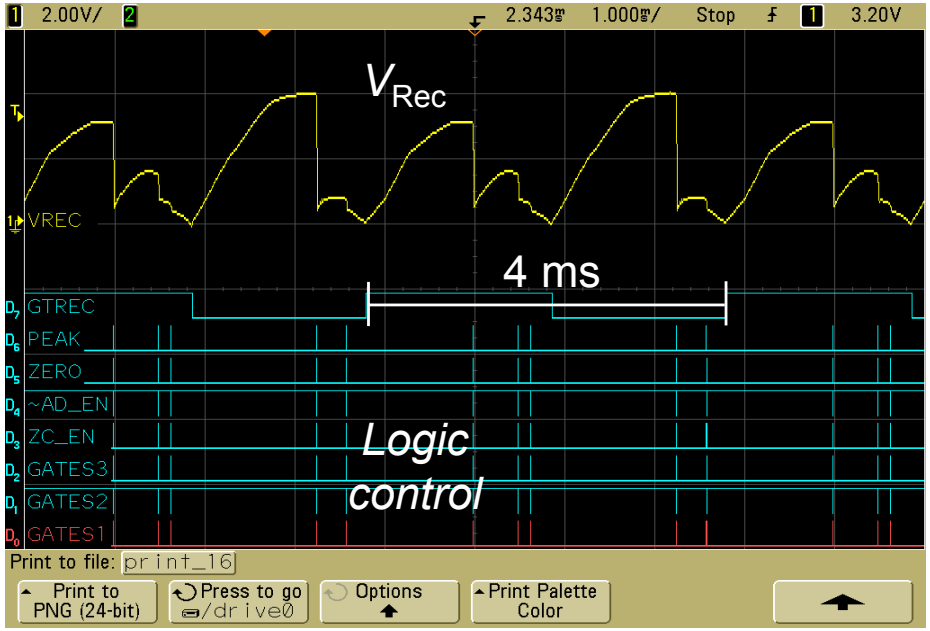


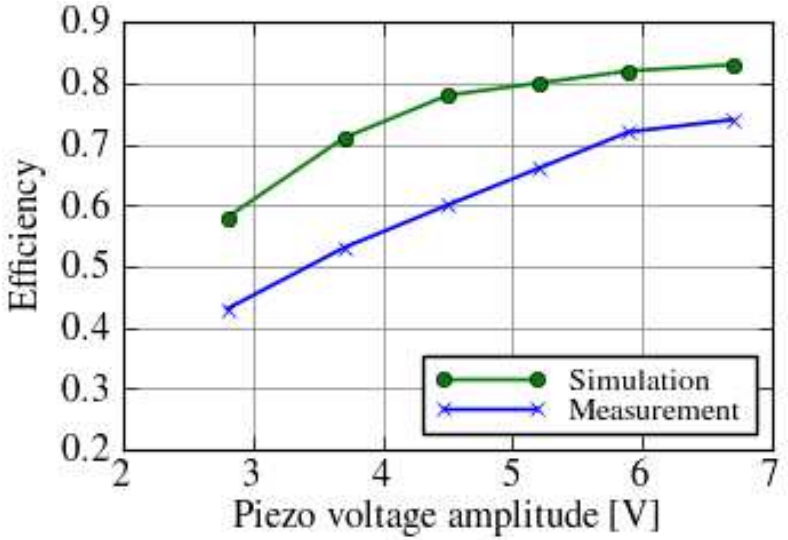
Chip Microphotograph

- Process: 0.35 µm with high voltage option
- Active area: 0.92 mm²



Simulation vs. Measurement Results



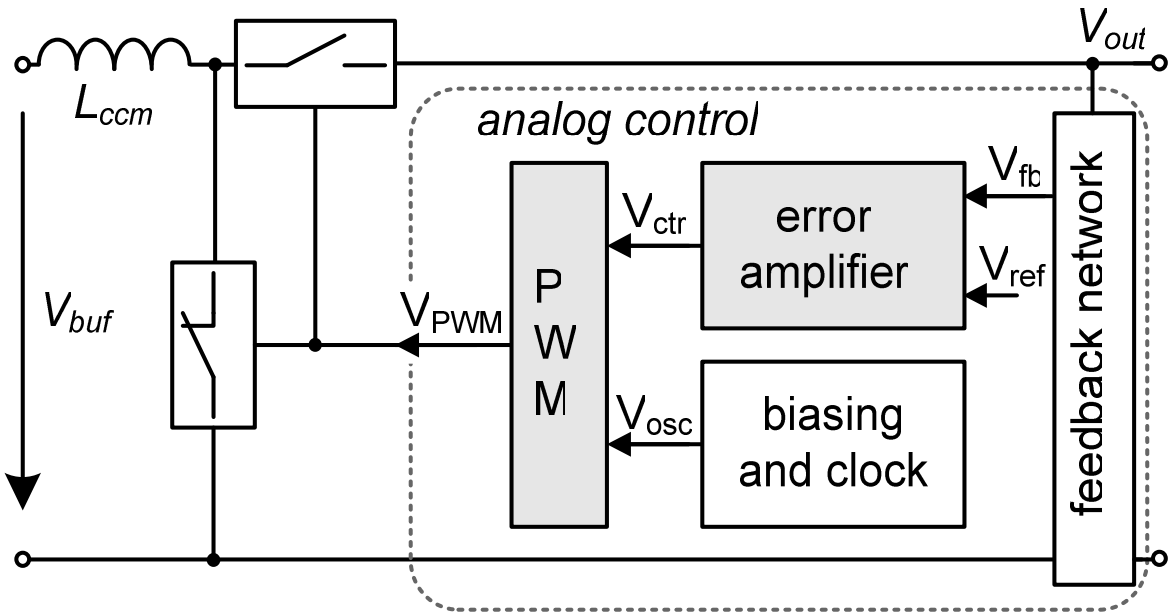


Parameters:
L=1mH, V_B=2V, C_P=12nF,
R_P=800kΩ, f_P=250Hz

- Proper peak detection for varying V_P
- Measured efficiency lower than simulated due to nonlinear parasitic losses which are not modelled

Chip specifications		
	Simulation	Measurement
Battery voltage V_B	1.3V … 3.5V	1.3V … 2V
Average power consumption	2.5µW	tbd
Piezo voltage amplitude V_P	1.4V … 7V	1.5V … 7V
Piezo frequency f_P	50Hz … 1000Hz (ca.)	tbd

DC/DC Converter - Basic Building Blocks



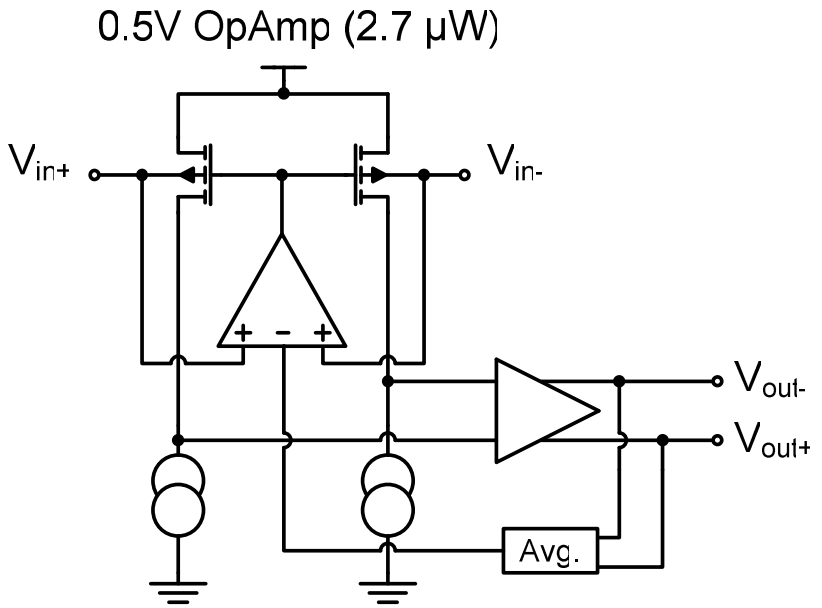
- Basic building blocks
  - Error amplifier
  - Pulse-width modulator
  - Voltage reference
  - Power-switch driver
- Operation conditions

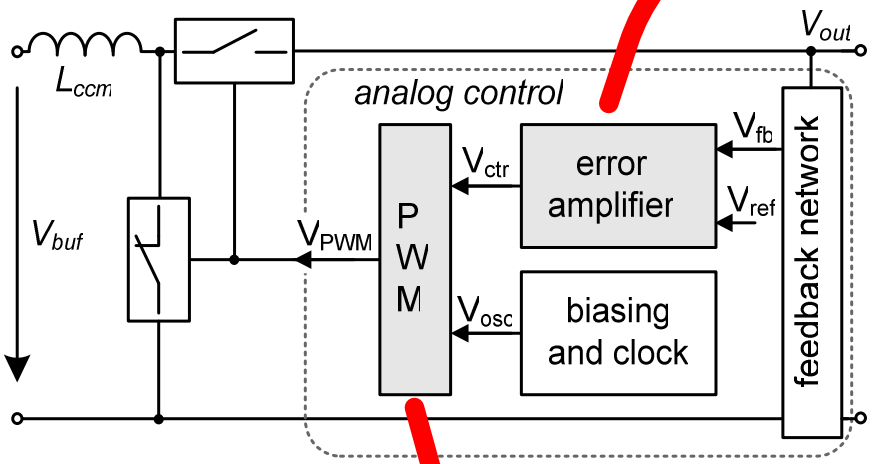
V_{DD} range	0.5 – 3.3 V
Power Loss	some 10 µW
Load Current	50 µA – 50 mA
Conv. range	0.5 ⟶ 3.3 V

- Designing energy-efficient low-voltage circuits
  - Sub-threshold operation
  - Bulk-driven and common-gate amplifiers
  - Creation of an *ultra-low voltage analog library* (IMTEK A_Cells)

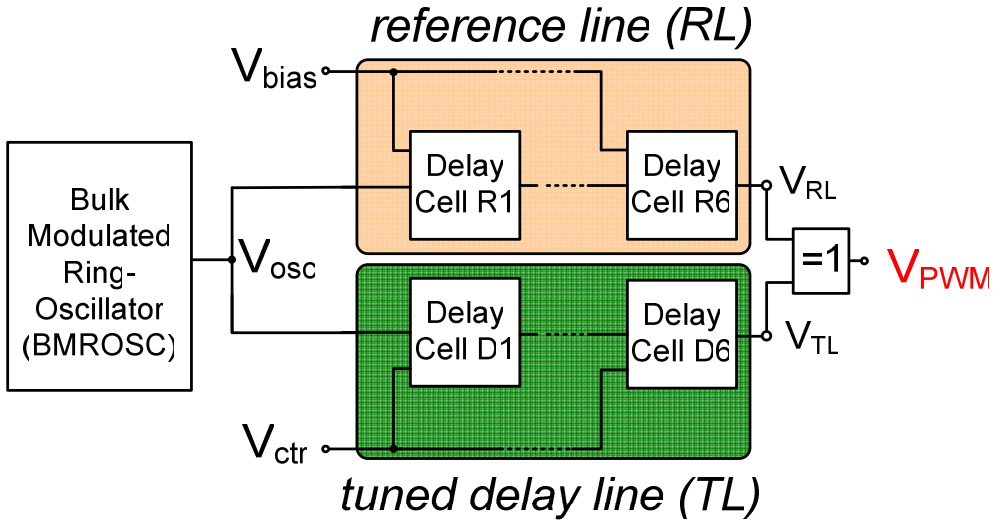
DC/DC Converter - Basic Building Blocks

- Bulk-driven input stage
- No tail: 2-stacked transistors only
- Biasing and feedback

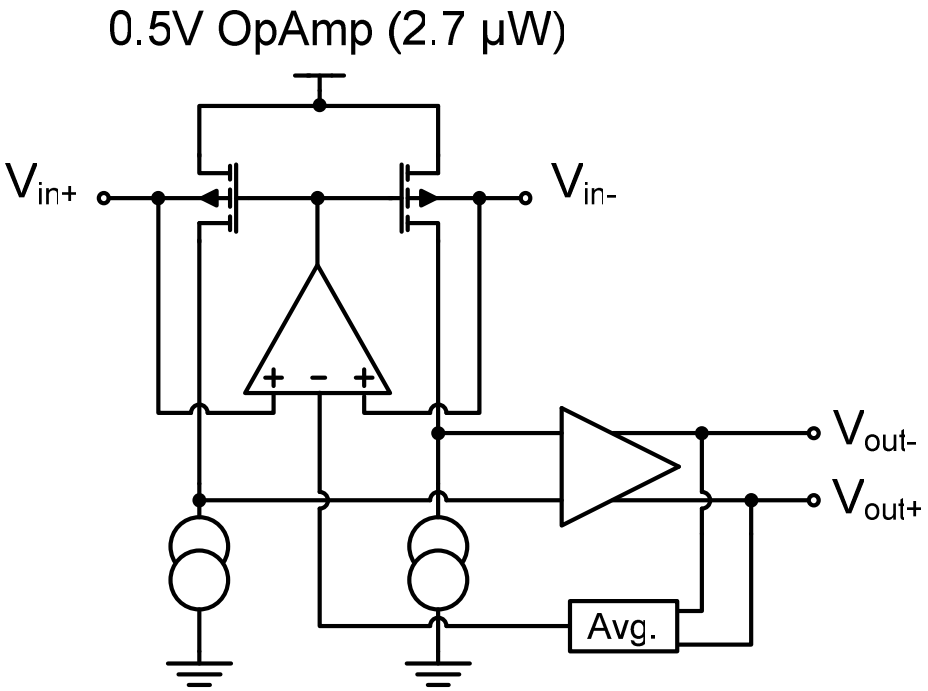


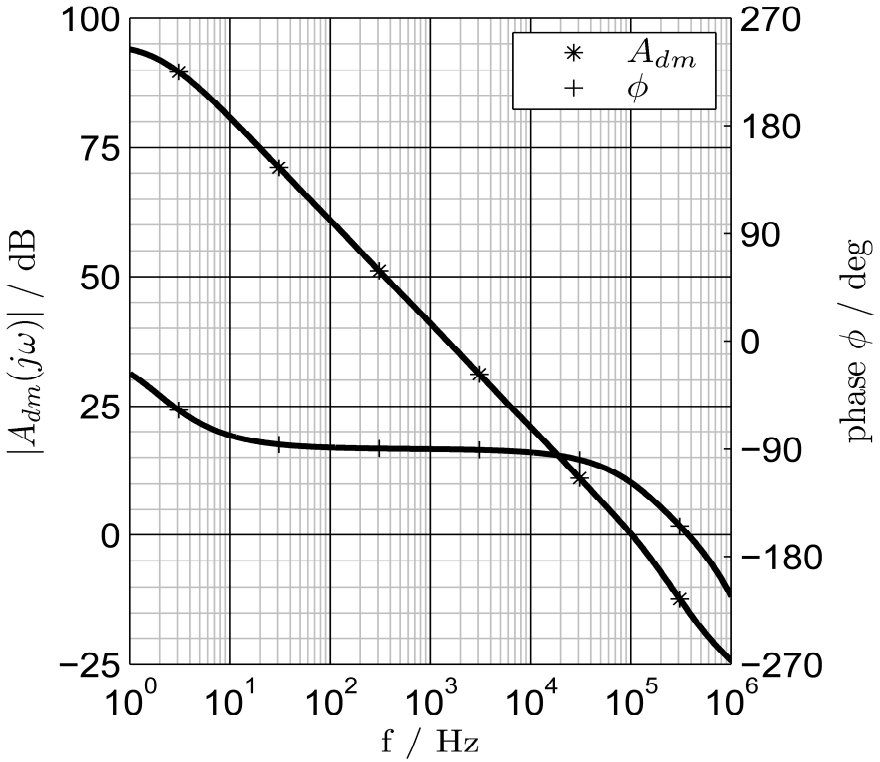


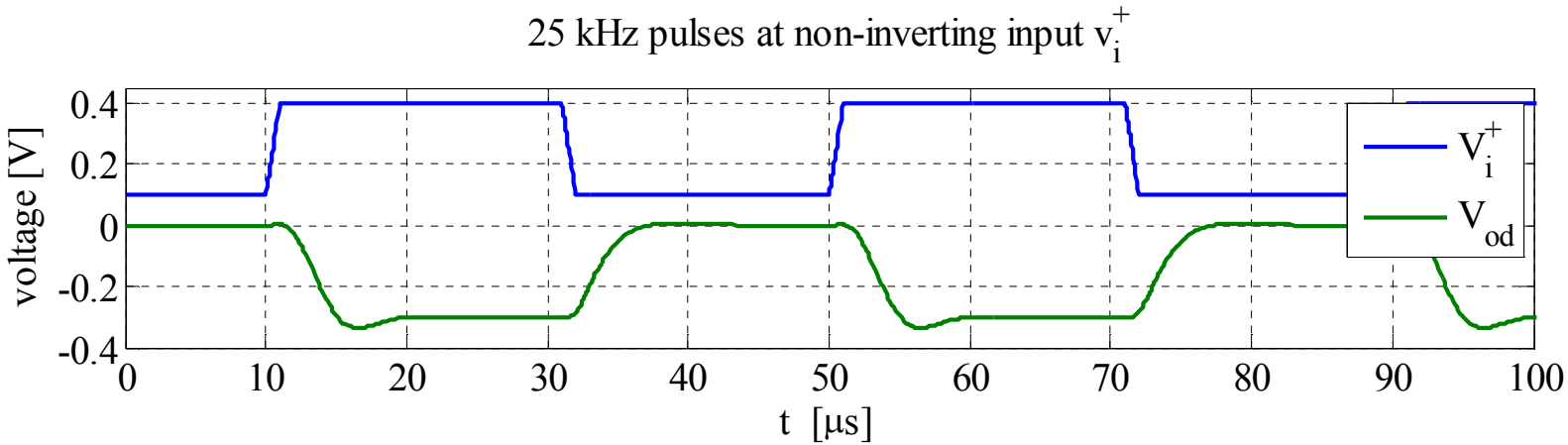
- Comparator-less PWM
- Tuned delay line modulation
- Bulk-driven inverters



Low-Voltage OpAmp







Performance Review

Parameter (V_{DD} = 0.5 V)	Fully Differential[4]	Single Ended[4]	Kinget[1,5]
DC Gain	93 dB	90 dB	48 dB
GBW, C_L = 10 pF	100 kHz	100 kHz	2.4 MHz[2]
PM, C_L = 10 pF	60°	60°	45°[2]
CMRR @ DC	50 dB	50 dB	-
PSRR @ DC	50 dB	50 dB	-
Inp. ref. noise (@100 Hz)	500 nV/√Hz	600 nV/ √Hz	220 nV/ √Hz[3]
Power P	2.7 µW	1.7 µW	100 µW
GBW·C_L/P for PM = 45°	0.48	0.97	0.48

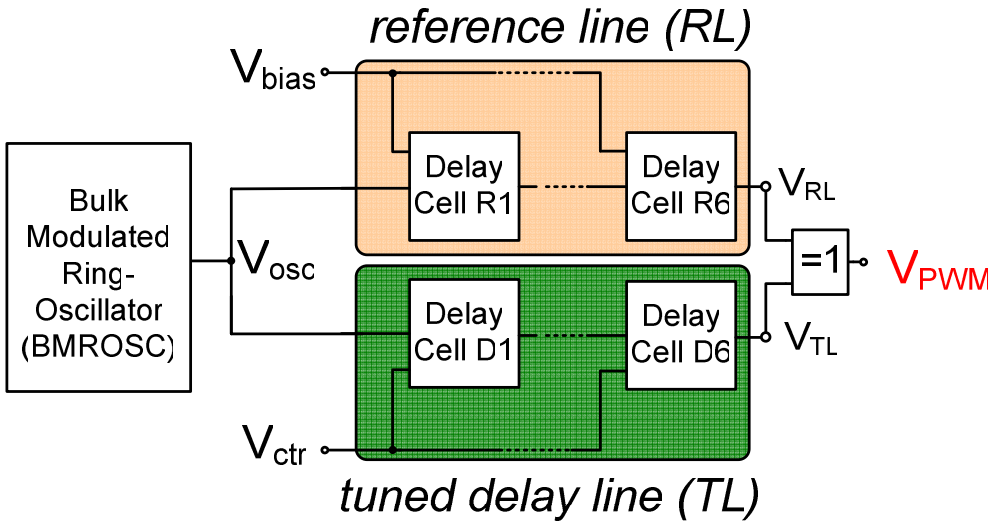
[1]Shouri Chatterjee, Yannis Tsividis, and Peter Kinget. 0.5-V analog circuit techniques and their application in OTA and Filter design. *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, 40(12), 2005.

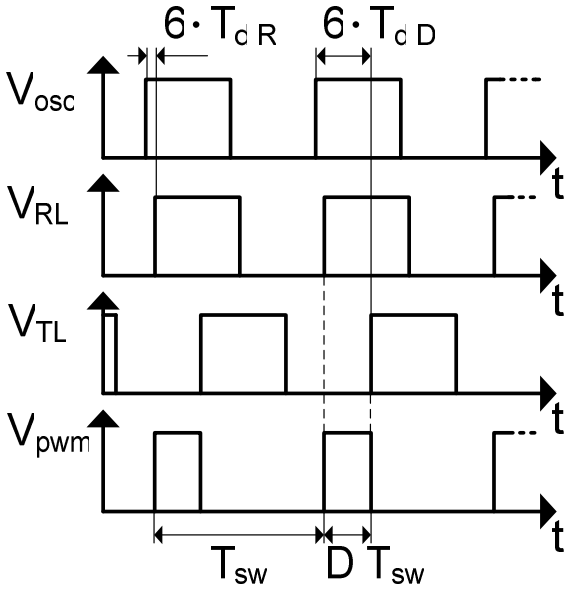
[2]C_L = 20 pF

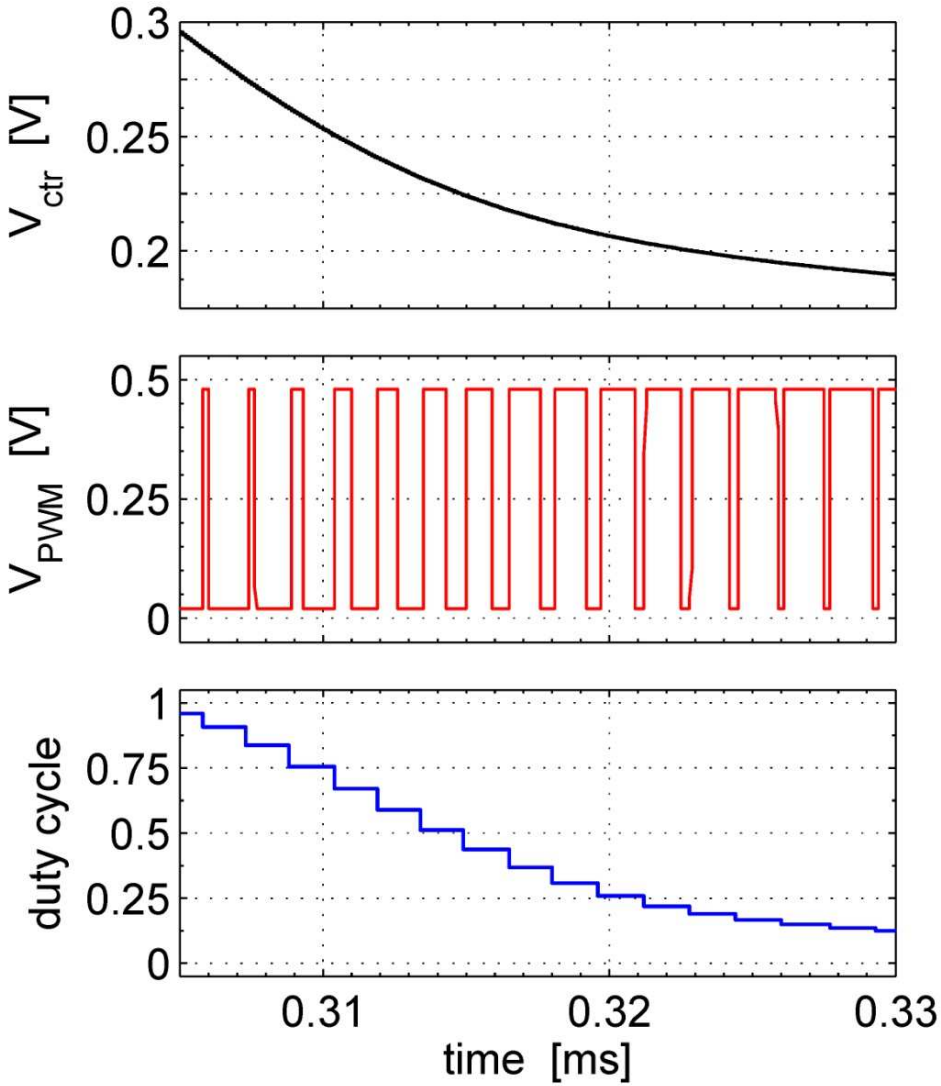
[3]@ 10 kHz

[4]0.35 µm process [5]0.18 µm process

Delay Line - Pulse Width Modulation

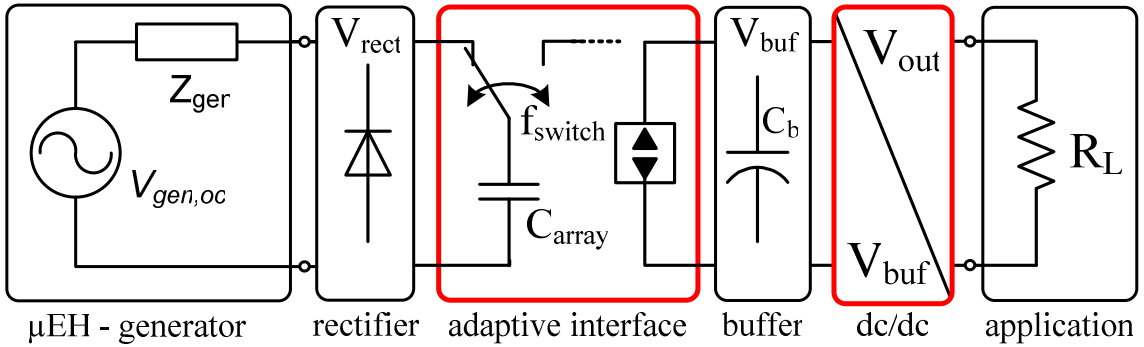






Conclusion

- Low-Voltage Rectification w/o single poly FG transistors
- Adaptive Interface on Chip
  - Measured enhanced impedance matching with charge control
  - Measured decoupling of buffer voltage and generator voltage



- Building Blocks for DC/DC conversion
  - Delay-based PWM modulation
  - Load adaptive power switch segmentation
- Reduced Supply requirements
  - Less Supply Voltage – high supply voltage flexibility (0.5 – 3.3 V)
  - Low-power consumption

Conclusion

- Two-stage power processing
  - Rectification and adaptive interface for efficient harvesting
  - Ultra-low-power DC/DC converter for stable output voltage
- Adaptive interfaces for inductive and piezoelectric generators
  - Decoupling of buffer and generator
  - Load impedance matching
- Building Blocks for DC/DC conversion
  - 0.5 V amplifier
  - Delay-based PWM modulation
- Reduced Supply requirements
  - Less Supply Voltage – high supply voltage flexibility (0.5 – 3.3 V)
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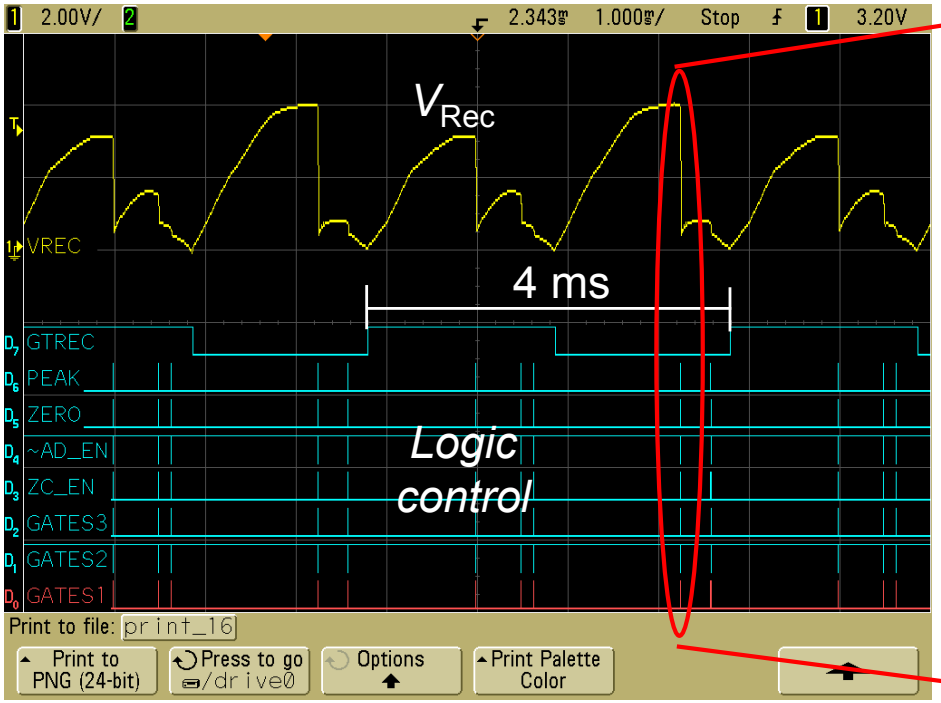
Thank you for your attention.

Measurement Results

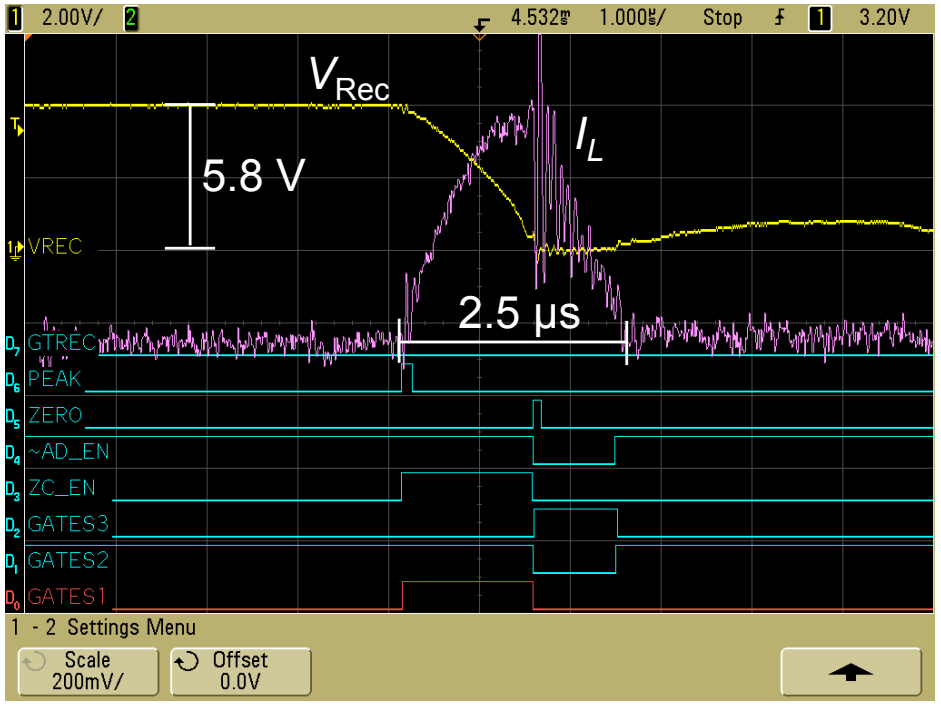
Several periods



Rectifier
Peak
Zero

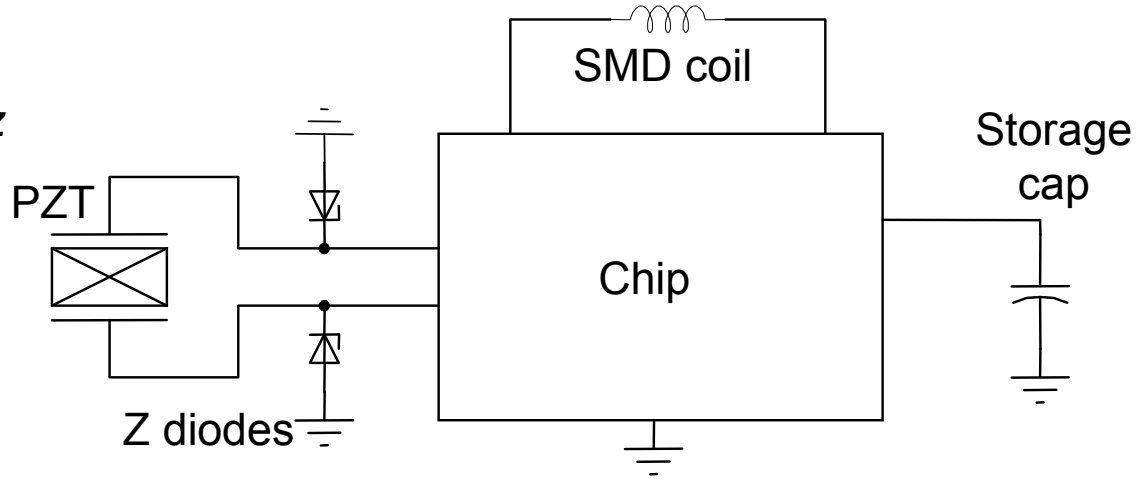
GateS3
GateS2
GateS1

One transfer process



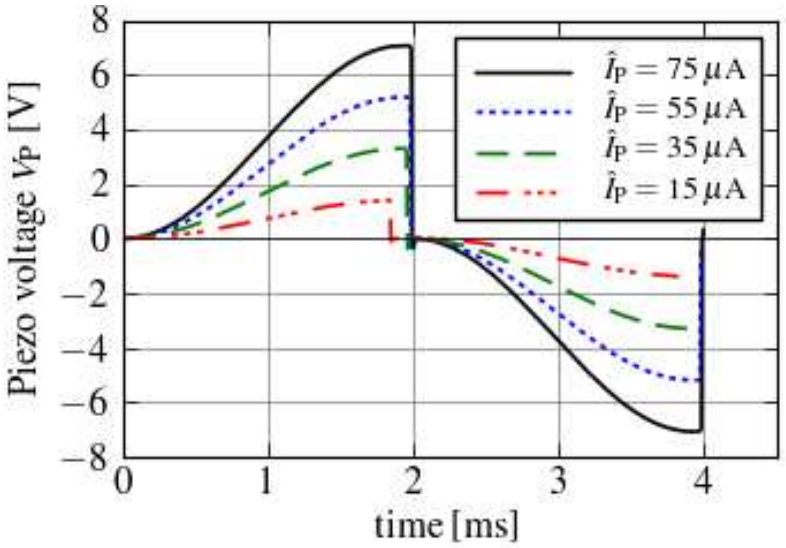
PZT bending generator Q220-A4-103YB (Piezo Systems Inc.), sinusoidal shaker excitation with 40µm amplitude and 250Hz

- Proper peak detection
- Proper logic control
- Two peaks per half period due to low R_P

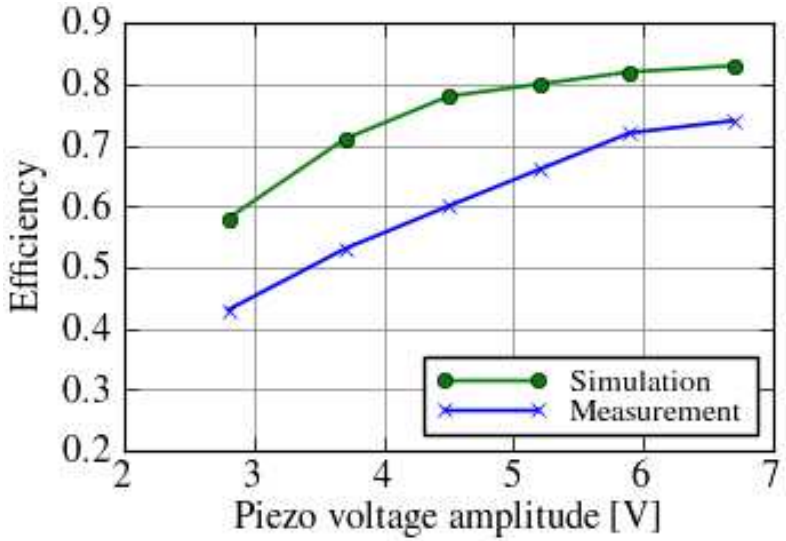


Simulation vs. Measurement Results

Simulation



Simulation & Measurement



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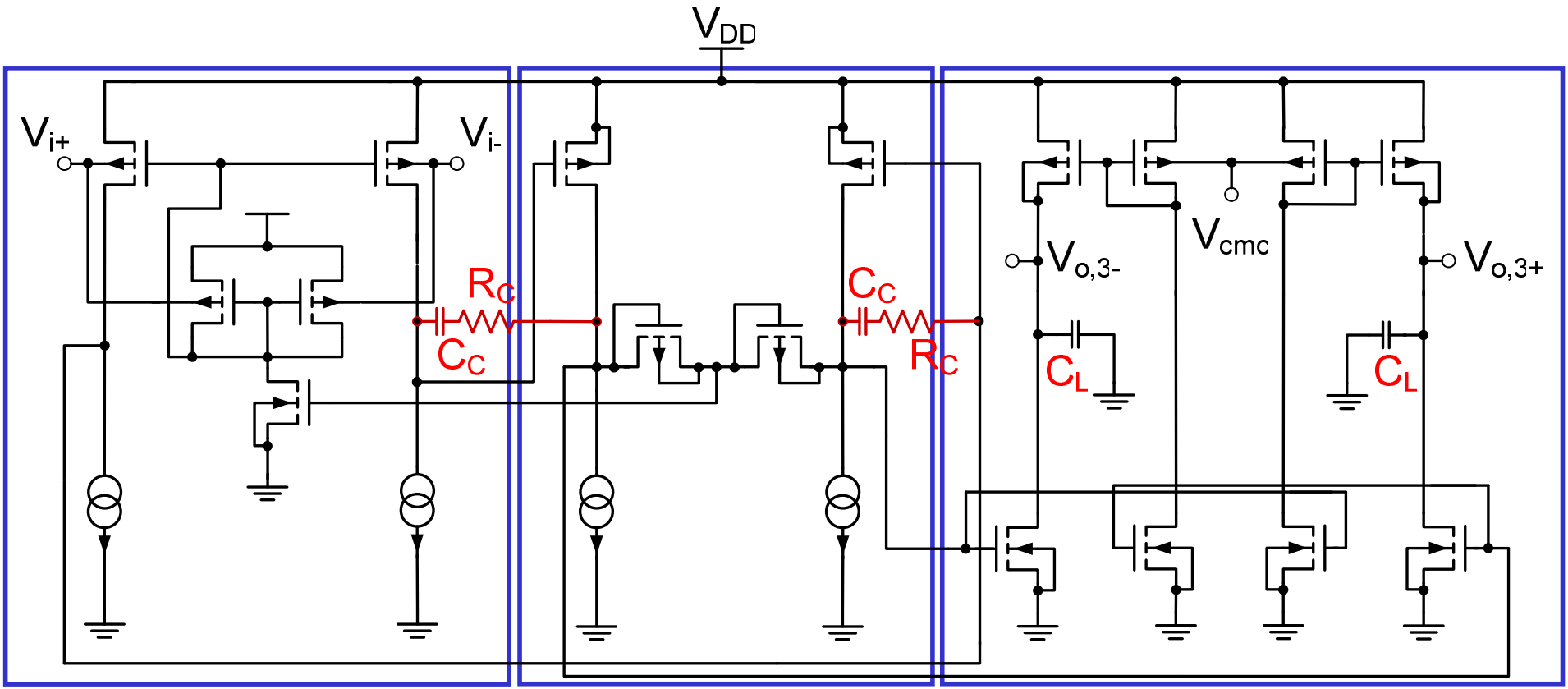
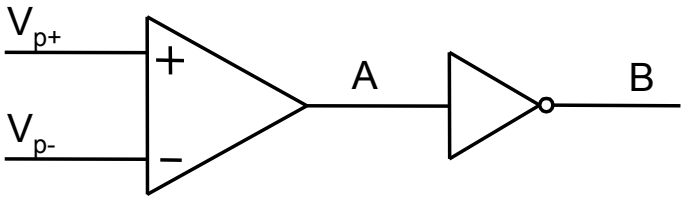
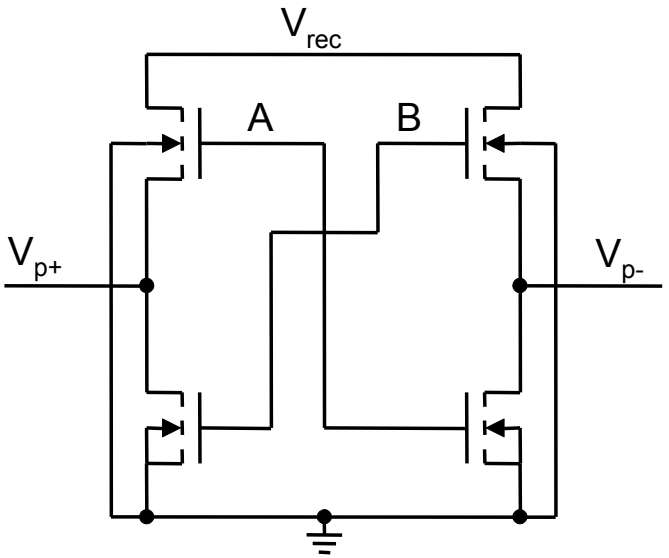
Error Amplifier

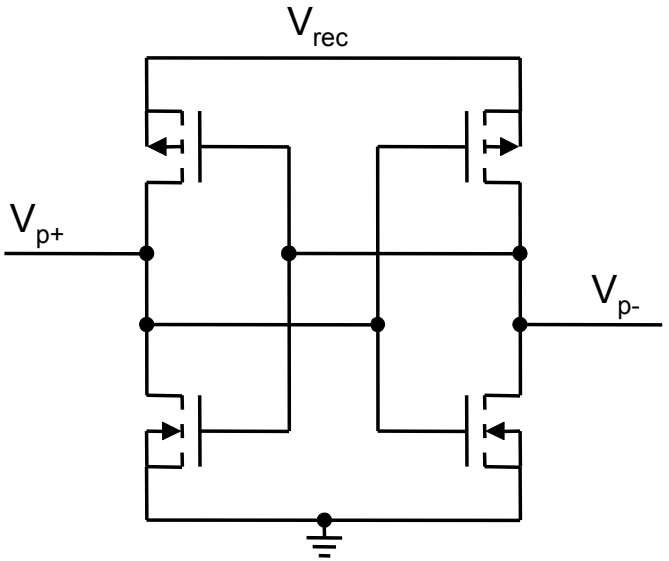
- Bulk – Driven Amplifier
- 3 – stage amplification
  - high unity-gain bandwidth (200kHz)
  - high gain (91 dB)
  - low output resistance
- Low power (5.4 µA – 2.7 µW)
- Low voltage (> 0.5 V)
  - Bulk-Source voltage limit
  - internal supply control (0.5 V)



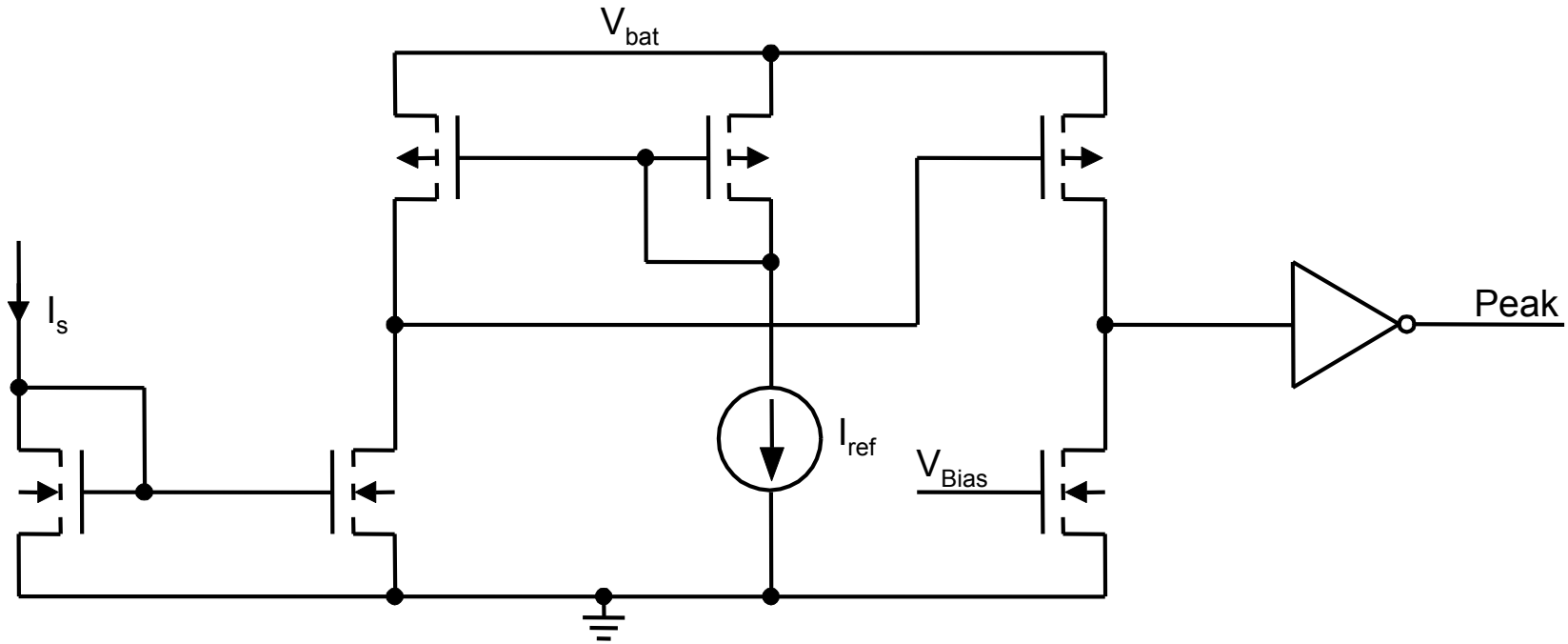
CMOS rectifier



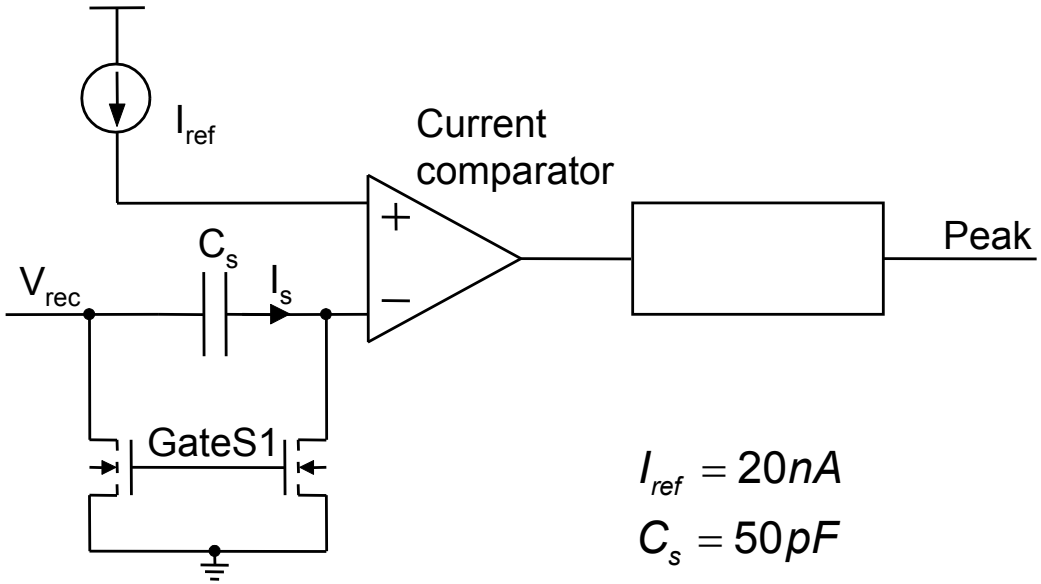


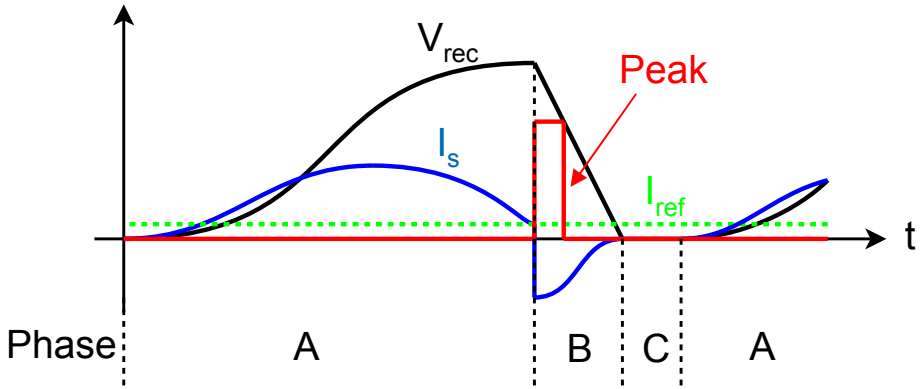


Current comparator



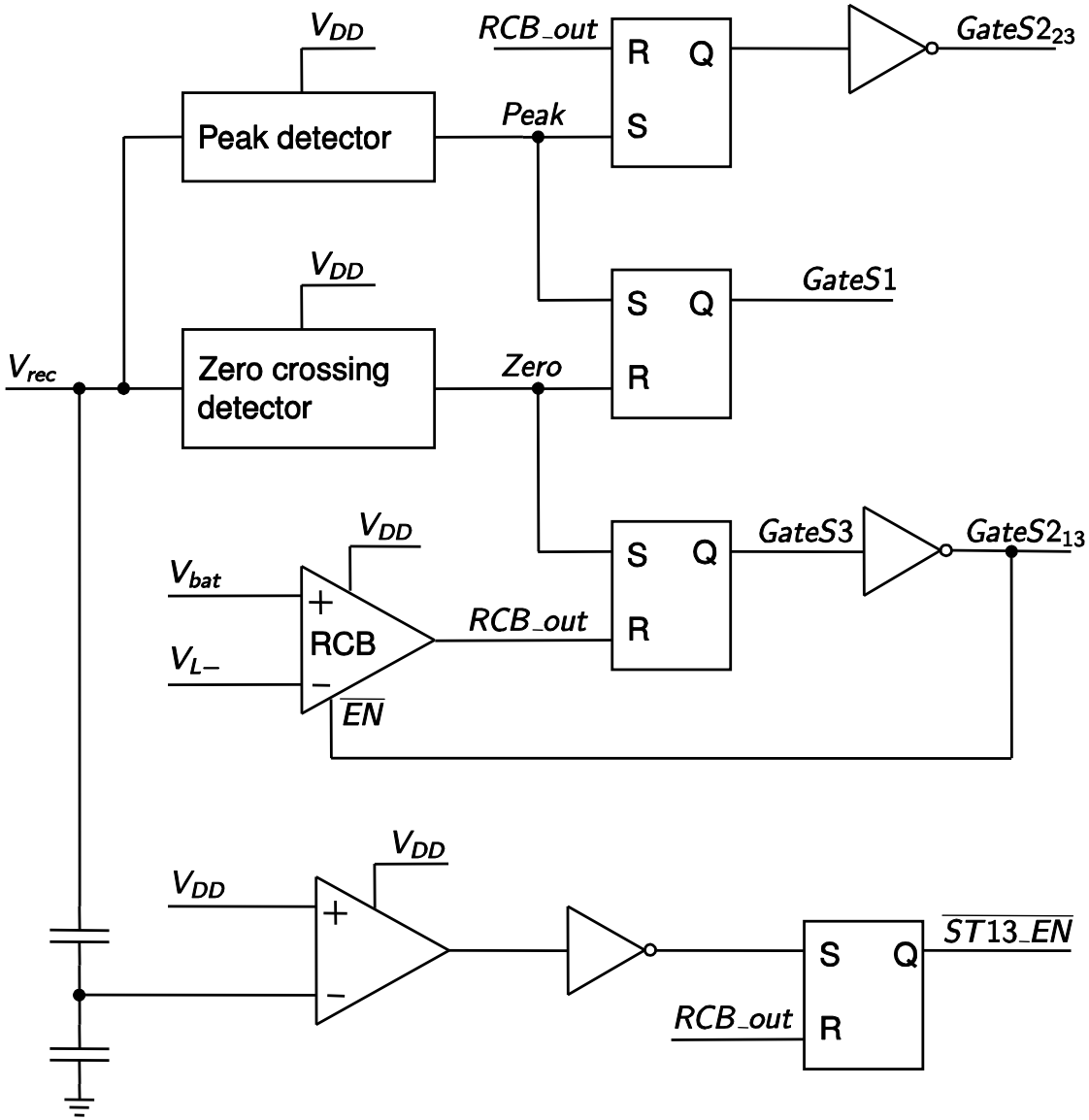
Peak detector





- Principle: Voltage-to-current conversion
- Series capacitor C_s is charged with I_s while V_{rec} rises
- When I_s falls below constant current I_{ref}, a peak pulse is generated, initiating transfer process
- After rising edge of peak pulse, C_s is discharged to be prepared for next cycle

HV circuit – Control circuit



HV circuit – Main